DEVELOPMENT OF INDIUM ARSENIDE QUANTUM WELL ELECTRONIC CIRCUITS

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DEVELOPMENT OF INDIUM ARSENIDE QUANTUM WELL

ELECTRONIC CIRCUITS

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SUMMARY

This dissertation focuses on the development of integrated circuits that employ InAs quantum well electronic devices. There are two InAs quantum well electronic devices studied in this work, the first being the pseudomorphic InAs/$In_{0.53}Ga_{0.47}As$/AlAs RTD grown on an InP substrate, and the second being the InAs/AlSb HEMT. Because of there is no semi-insulating substrate near the InAs lattice constant of 6.06 Å, this work subdivides the devices into two categories by the integration method employed to realize circuits: monolithic integration or hybridization. In the case of hybrid RTD circuits, a thin-film integration method was developed to integrate InAs/$In_{0.53}Ga_{0.47}As$/AlAs RTDs to prefabricated CMOS circuits, and this technique was employed to demonstrate a novel RTD-CMOS comparator. Similar InP-based RTDs can be integrated with InP-based HEMTs in monolithic RTD-HEMT integrated circuits, and in this work elementary microwave circuit components were characterized that co-integrate InP-based tunnel diodes with HEMTs. In the case of the InAs/AlSb HEMT, the monolithic approach grows the HEMT on a metamorphic buffer on a GaAs substrate. A hybrid transferred-substrate back-gated InAs/AlSb HEMT that would allow the device to reach its ultimate performance limits is beyond the scope of this work, but can be developed in the future when the monolithic HEMT has reached its limits.

This dissertation is comprised of eight chapters. The first provides an introduction to InAs quantum well electronic devices, and outlines the basic circuit integration methods available. The next three chapters focus on the development of hybrid RTD-CMOS circuits. The second chapter summarizes the RTD characteristics

and circuit designs considered, and the third chapter covers the RTD-CMOS thin-film hybridization process that yielded the first simple RTD-CMOS integrated circuit demonstrations. The fourth chapter details the development of a next-generation RTD fabrication process that addresses the limitations of the baseline process to reduce parasitic capacitances and allow for multiple RTDs to be transferred to the CMOS chip. The fifth chapter briefly summarizes the characterization of MMICs in QMMIC technology that integrates InP-based tunnel diodes monolithically with HEMTs. The sixth and seventh chapters are devoted to the InAs/AlSb HEMT. The sixth chapter covers the material and process development of the InAs/AlSb HEMT that was necessary to make the transition from laboratory device demonstration to a specialized low-power MMIC technology. The seventh chapter describes and analyzes the remarkable RF small-signal and noise characteristics of these MMIC-compatible HEMTs. The significant effects of impact-ionization due to the 0.36 eV bandgap of InAs are given special attention. The eighth and final chapter discusses the conclusions, relevance, and possible future research in the technical areas studied in this work.

CHAPTER 1

INTRODUCTION TO INDIUM ARSENIDE ELECTRONICS

1.1. The Merits of Indium Arsenide for Electronic Applications

The appeal of InAs for high speed electronic devices derives from its inherent semiconductor properties, as it does for other compound semiconductor materials such as the more established GaAs and InP-based semiconductors. More specifically, the electronic band structure of InAs allows for faster electron transport on account of its lower effective mass in the Γ-valley relative to other III-V semiconductors commonly in use. Values of the key electron transport parameters of InAs are listed in Table 1.1, with the corresponding values for GaAs, pseudomorphic $In_{0.25}Ga_{0.75}As$ on GaAs, and InP-matched $In_{0.53}Ga_{0.47}As$ for comparison. Along with the reduction in band gap from 1.42 eV to 0.36 eV, the effective mass decreases from $0.067m_o$ to $0.023m_o$ as the indium composition of $In_xGa_{1-x}As$ increases from 0 to 100%. The decrease in effective mass directly impacts the low-field mobility of each semiconductor material, as evidenced by the increase in 300 K electron mobility from 4,600 $cm^2/V\text{-}s$ in GaAs to 16,000 $cm^2/V\text{-}s$ in InAs doped at $N_d = 1 \times 10^{17}$ cm^{-3}. The improved electron mobility in turn lowers access resistances in transistors and diodes that ultimately limit the device operating speed.

Table 1.1 $In_xGa_{1-x}As$ semiconductor properties

	GaAs	Pseudo-morphic $In_{0.25}Ga_{0.75}As$	$In_{0.53}Ga_{0.47}As$	InAs
Band Gap (eV)	1.42	1.21	0.73	0.36
Electron Effective Mass ($\times m_o$)	0.067	0.061	0.041	0.023
Γ-L Valley Separation (eV)	0.28	0.42	0.55	0.72
Peak Electron Velocity (cm/s)	2.0×10^7	$\approx 2.0 \times 10^7$	2.7×10^7	4.0×10^7

In transistors, it is the peak or saturated electron velocity that limits the electron transit times. On account of its relatively large energy separation between the Γ- and L-valleys in the conduction band, electrons in InAs can acquire a higher kinetic energy before populating the L-valley, which has a much higher effective mass. As a consequence, InAs exhibits a high electron peak velocity, with Dobrovolskis *et al.* measuring an electron velocity of 4.0×10^7 cm/sec at an electric field of 0.5 kV/cm at 77 K [1]. This value represents a 50% increase over the peak velocity of $In_{0.53}Ga_{0.47}As$, and doubles that of GaAs. Further, because the Γ-L valley separation (0.72 eV) is larger than the band gap in InAs (0.36 eV), a theoretical investigation by Brennan and Hess predicts electron drift velocities over 1×10^8 cm/sec due to the confinement of hot electrons in the Γ-valley by impact ionization [2].

1.2. Indium Arsenide Quantum Well Electron Devices: the Resonant Tunneling Diode and High Electron Mobility Transistor

For the discussion here, the InAs quantum well (QW) electronic devices are divided into two broad classes: (1) nanoelectronic devices that derive their characteristics from electron wave effects in a quantum heterostructure, and (2) conventional electronic devices that derive their characteristics from electron drift and diffusion. The most practically applicable nanoelectronic device is the InAs quantum well resonant tunneling diode (RTD), while the most useful conventional device is the InAs single quantum well (SQW) high electron mobility transistor (HEMT). Both the InAs RTD [3], [4] and the InAs/AlSb HEMT [5]-[8] have been demonstrated in research labs and can operate at room temperature. In the case of the RTD, InP-based $In_{0.53}Ga_{0.47}As$/AlAs RTDs without an InAs subwell have already demonstrated switching speeds as low as 1.5 ps [9]. The addition of the InAs subwell to the RTD quantum well, with its lower conduction band energy and effective mass, is essential in realizing low-power RTDs, as will be explained in further detail in Section 1.2.1. Likewise, while the mature InP-based $In_{0.53}Ga_{0.47}As$/ $In_{0.52}Al_{0.48}As$ HEMT has demonstrated current gain cutoff frequencies of up to 472 GHz for a state-of-the-art HEMT with a 30 nm gate length [10], the InAs/AlSb has the immediate advantage of improved low-power operation due to its inherently superior electron mobility and confinement in the 2DEG, which results in lower drain saturation voltages. In Section 1.2.2, the electron transport properties of the InAs/AlSb 2DEG that allow it to offer the promise of enhanced speed-power performance in InAs-based HEMTs are discussed.

1.2.1. Reduced operating power: the advantage of InAs subwell RTDs

The resonant tunneling diode (RTD) has two intrinsic figures of merit: the peak-to-valley current ratio (PVCR) and the speed index. The PVCR is the ratio of the RTD peak current to the valley current, $PVCR = I_p / I_v$, where I_p and I_v are the peak and valley current, respectively. The peak current is reached when the voltage in the diode aligns the conduction band edge in one of the terminals to first electron resonance in the RTD quantum well. Past the peak voltage, the RTD enters the negative differential resistance (NDR) region, where the current drops dramatically until the terminal conduction band nears the second resonance. Figure 1.1 shows a representative double barrier resonant tunneling diode I-V characteristic, along with schematic band diagrams of the RTD (a) at zero bias, (b) at the peak, (c) past the peak, and (d) near the turn-on voltage of the second resonance.

The speed index, the second figure of merit for the intrinsic RTD is defined as the ratio of the peak current to the device capacitance near the peak voltage, i.e., $speed\ index = I_p / C$, and has units of A/pF, or equivalently V/ps. Due to the very short transit times of ballistic electrons through the quantum region of the device, RTD switching speed is limited by capacitive charging times, and the speed index indicates the upper limit of the device's switching speed.

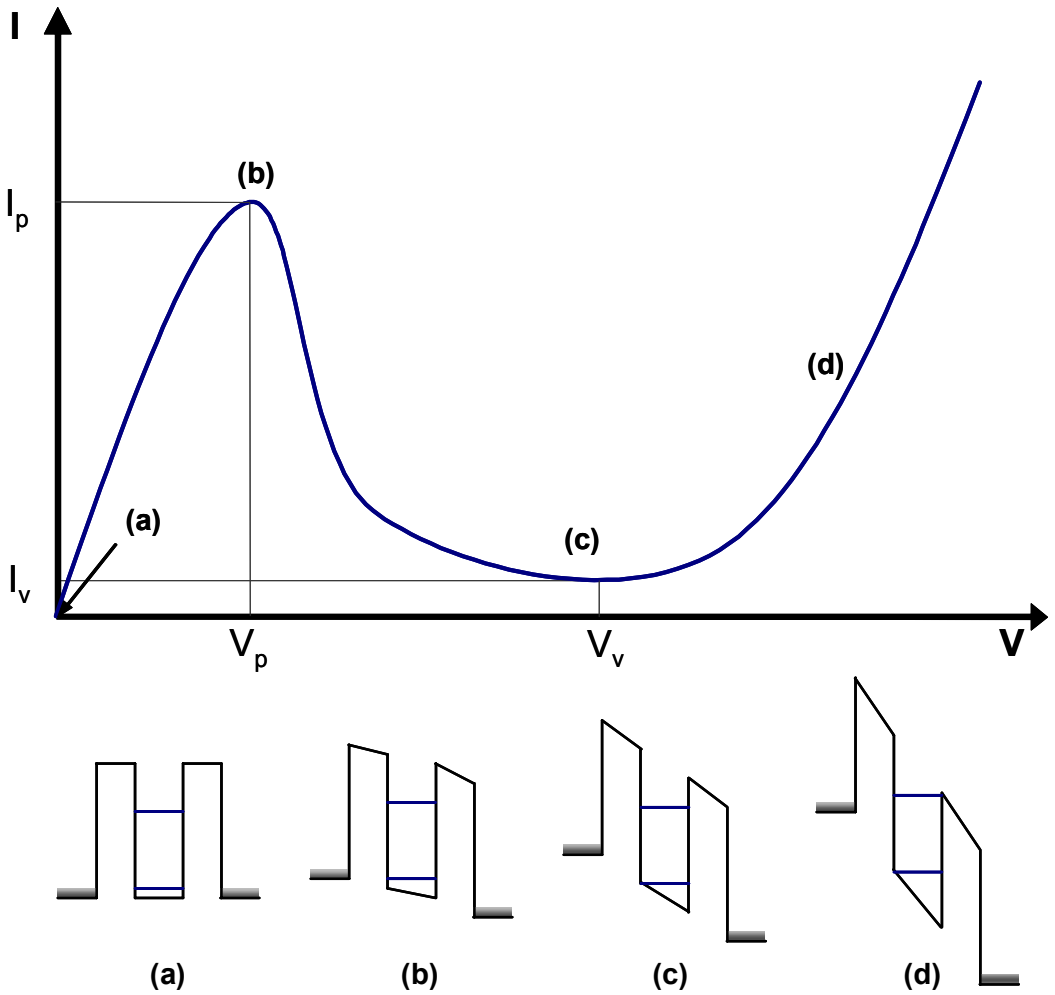


Figure 1.1 A representative current-voltage plot of a double-barrier RTD. The inset band diagram schematics show the energy in the terminals relative to the first and second resonance energies.

The highest performance RTDs in terms of reported peak current density (680 kA/cm^2 [9]), PVCR (53 [11]), and switching speed (1.5 ps [9]) have been fabricated on InP substrates. The earliest such RTDs were strictly lattice-matched using $In_{0.53}Ga_{0.47}As$ for the quantum well and $In_{0.52}Al_{0.48}As$ for the barriers. By replacing the lattice-matched $In_{0.52}Al_{0.48}As$ barriers with pseudomorphic AlAs barriers, it was found that the peak-to-valley ratio at 300 K could be increased from 5.5 to 14 [3], and peak current densities as high as 460 kA/cm^2 were reported with a 300 K PVCR of 4 [12]. The PVCR was further improved from 17 to 30 in otherwise identical structures by introducing a pseudomorphic InAs subwell to the $In_{0.53}Ga_{0.47}As$/AlAs RTD [13], and InAs/$In_{0.53}Ga_{0.47}As$/AlAs RTDs were later reported with a PVCR of 53 [11]. The lower electron effective mass of the InAs subwell relative to $In_{0.53}Ga_{0.47}As$ increases the PVCR by increasing the energy separation between the first and second resonances in comparison to an otherwise identical $In_{0.53}Ga_{0.47}As$/AlAs RTD without the InAs subwell.

Table 1.2 The RTD layer structures used in the simulations

Layer Name	(a) InAs Notch QW Composition	(b) $In_{0.53}Ga_{0.47}As$ QW Composition	Thickness (Å)	Doping (cm^{-3})
Terminal 1	$In_{0.53}Ga_{0.47}As$	$In_{0.53}Ga_{0.47}As$	100	1E18
n^+ contact	$In_{0.53}Ga_{0.47}As$	$In_{0.53}Ga_{0.47}As$	100	1E18
Spacer	$In_{0.53}Ga_{0.47}As$	$In_{0.53}Ga_{0.47}As$	41	1E15
Barrier	AlAs	AlAs	25	1E15
QW spacer	$In_{0.53}Ga_{0.47}As$	$In_{0.53}Ga_{0.47}As$	9	1E15
QW notch	InAs	$In_{0.53}Ga_{0.47}As$	27	1E15
QW spacer	$In_{0.53}Ga_{0.47}As$	$In_{0.53}Ga_{0.47}As$	9	1E15
Barrier	AlAs	AlAs	25	1E15
Spacer	$In_{0.53}Ga_{0.47}As$	$In_{0.53}Ga_{0.47}As$	41	1E15
n^+ contact	$In_{0.53}Ga_{0.47}As$	$In_{0.53}Ga_{0.47}As$	100	1E15
Terminal 2	$In_{0.53}Ga_{0.47}As$	$In_{0.53}Ga_{0.47}As$	100	1E18

To illustrate the benefit of the inclusion of the InAs subwell, a simple simulation was performed using the nanoelectronics modeling program NEMO [14], using the two baseline $In_{0.53}Ga_{0.47}As$/AlAs RTD structures described in Table 1.2. The RTD was modeled using parabolic bands and parabolic densities of states, with a Thomas-Fermi potential model used to calculate resonances. The J-V calculations were performed using a fully self-consistent potential, and no scattering effects were included because electron scattering does not significantly affect the overall current at voltages below the peak voltage. As shown in Figure 1.2(a), the lower effective mass of the InAs/$In_{0.53}Ga_{0.47}As$ composite quantum well lowers the energy of the first resonance, while increasing the energy of the second resonance relative to the $In_{0.53}Ga_{0.47}As$ quantum well RTD. The inclusion of the InAs subwell increases the energy separation between the second and first resonances (ΔE_{21}) from 0.55 eV to 0.88 eV. The PVCR thereby is improved because the primary contribution to the valley current at room temperature in the $In_{0.53}Ga_{0.47}As$/AlAs RTD is expected to be the tunneling current through the second resonant state. In addition, as is evident in Figure 1.2(b), the InAs subwell RTD exhibits a reduced peak voltage of 0.27 V compared with 0.60 V for the all-$In_{0.53}Ga_{0.47}As$ QW RTD, and is expected to have an equal or higher turn-on voltage for the excess current in the second PDR region. Table 1.3 lists the simulation results of the two devices at zero bias and when biased at the peak.

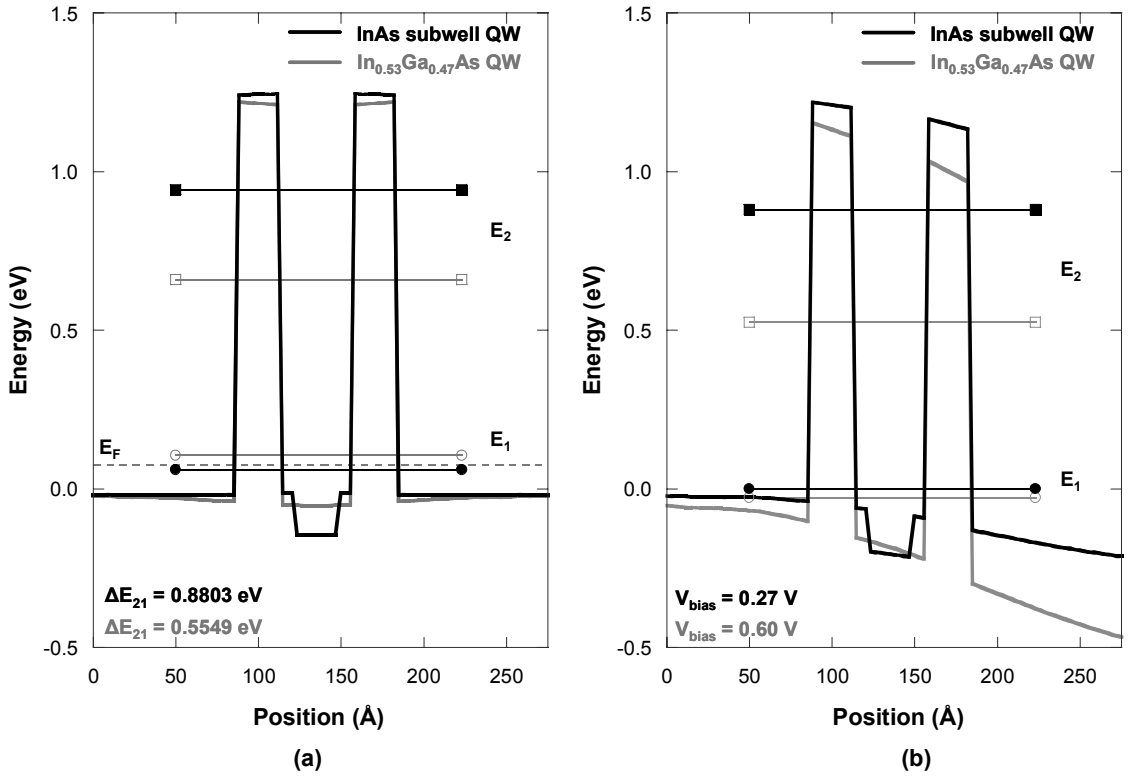


Figure 1.2 (a) The zero-bias conduction band profile and electron resonances in otherwise identical $In_{0.53}Ga_{0.47}As$/AlAs RTDs with and without the InAs subwell. (b) A plot of the same devices when biased just below their respective peaks.

Table 1.3 Simulated characteristics of the $In_{0.53}Ga_{0.47}As$/AlAs RTD (a) with and (b) without an InAs subwell

Quantity	(a) InAs Notch QW	(b) $In_{0.53}Ga_{0.47}As$ QW
E_1 (zero bias)	0.0615 eV	0.1058 eV
E_2 (zero bias)	0.9418 eV	0.6607 eV
ΔE_{21} (zero bias)	0.8803 eV	0.5549 eV
Voltage at peak	0.27 V	0.60 V
Current density at peak	332.3 A/cm^2	723.4 A/cm^2
E_1 (biased for peak)	0.0001 eV	-0.0277 eV
E_2 (biased for peak)	0.8798 eV	0.5257 eV
ΔE_{21} (biased for peak)	0.8797 eV	0.5534 eV

The improved PVCR in the InAs subwell RTD translates directly into lower power consumption because a loaded RTD operating its stable point in the higher PDR region will consume a static current of at least I_v. While increasing the barrier thicknesses will also lower I_v, it will not improve the speed-power product because I_p will also be lowered by at least an equal factor, which proportionally degrades the RTD speed index. The second way that the InAs subwell lowers the RTD power dissipation in circuit applications is through the reduction of the peak voltage. In comparator and other triggering applications, for example, the RTD is biased just below the peak current so that a small input current switches the RTD. In this case the DC power consumption will be reduced by operating at the lower voltage possible in the InAs subwell RTD. Also, in many proposed RTD-CMOS circuits, the RTD's stable operating voltage in the first PDR region, where $V < V_p$, need to be well below the nMOSFET's threshold voltage, which is typically near 0.7 V, with the stable operating voltages in the second PDR region being well above the threshold to provide higher ON-OFF gain. For these reasons, the strain-compensated InAs/$In_{0.53}Ga_{0.47}As$/AlAs RTD was selected as the optimal structure for RTD-CMOS integration.

1.2.2. Electron transport in the InAs/AlSb 2DEG

The InAs/AlSb HEMT, like its counterparts in the GaAs and InP material systems, derives its high speed performance from the inherently fast electron transport properties of the channel semiconductor, as opposed to the modern silicon FETs for which advanced device engineering dictates the transistor performance. As was discussed in Section 1.1, the low effective mass of InAs ($m_e = 0.023m_o$) permits the realization of InAs quantum wells with very high electron mobilities. Of greater

importance in a HEMT is the improvement in the peak and saturation electron velocities in InAs over those of GaAs and $In_{0.53}Ga_{0.47}As$ which increases the maximum possible transistor speed by lowering electron transit times through the channel. The fundamental impact of the electron velocity in the channel is expressed in formula for the intrinsic transconductance,

$$g_{mi} = C_{gs} v_e , \tag{1.1}$$

where g_{mi} is the intrinsic transconductance per unit gate width, C_{gs} is the specific gate-to-source capacitance (capacitance per unit area), and v_e represents the average electron velocity. This result in turn yields the dependence of the cutoff frequency f_τ on the electron velocity,

$$f_\tau \cong \frac{1}{2\pi} \frac{v_e}{L_g}, \tag{1.2}$$

where L_g is the gate length. The equality is approximate because this simplified formula neglects additional parasitic capacitances and resistances present in a practical HEMT. Because InAs has the highest electron velocity of any III-V semiconductor, an InAs-channel HEMT should be able to obtain the highest possible device speed at a given gate length.

An additional advantage is gained through the use of AlSb barriers because the nearly lattice-matched AlSb has a conduction band offset of 1.35 eV relative to InAs [15], the largest conduction band offset of any pair of (nearly) lattice-matched III-V semiconductors. Thus, the InAs/AlSb combination forms a very deep quantum well can hold a much higher electron density than a GaAs/AlGaAs and InGaAs/InAlAs HEMT. Experience in GaAs PHEMTs and InP-based HEMTs has shown that a high electron

sheet density is the most critical parameter in the realization of fast transistors. In fact, nearly all of the high frequency performance improvement of the InGaAs/AlGaAs PHEMT over the GaAs HEMT can be attributed to the higher modulation efficiency attributable to the deeper quantum well [16], since there is no significant change in the electron mobility or drift velocity. Comparisons of otherwise identical $In_{0.53}Ga_{0.47}As$/ $In_{0.52}Al_{0.48}As$ HEMTs have indicated that raising the channel sheet charge through delta-doping in the HEMT has increased the transistor's cutoff frequency and linearity [17]. The essential properties of the InAs/AlSb HEMT 2DEG are listed in Table 1.4, with those of the GaAs HEMT, GaAs PHEMT, and InP-based HEMT included for comparison. The Hall sheet charge and mobility represent the high end of published values for sheet charge density and mobility for each technology. The channel sheet conductivity for the heavily doped InAs/AlSb HEMT ($N_s = 8.0 \times 10^{12}$ cm^{-2}, $\mu = 19{,}000$ $cm^2/V\text{-}s$) [18] is four times that of an InP-based HEMT, demonstrating the potential for high speed operation at low drain voltages.

Table 1.4 Fundamental material properties of the HEMT 2DEG

	GaAs HEMT	GaAs PHEMT	InP HEMT	InAs HEMT
Channel Composition	GaAs	$In_{0.25}Ga_{0.75}As$	$In_{0.53}Ga_{0.47}As$	InAs
Barrier Composition	$Al_{0.3}Ga_{0.7}As$	$Al_{0.3}Ga_{0.7}As$	$In_{0.52}Al_{0.48}As$	AlSb
Channel Band Gap (eV)	1.42	1.21	0.73	0.36
Conduction Band Barrier Height (eV)	0.26	0.37	0.52	1.35
Peak Electron Velocity (cm/s)	2.0×10^7	$\approx 2.0 \times 10^7$	2.7×10^7	4.0×10^7
2DEG Sheet Charge (cm^{-2})	1.2×10^{12}	2.5×10^{12}	3.5×10^{12}	8.0×10^{12}
2DEG Hall Mobility (cm^2/Vs)	6,000	6,600	9,500	19,000

The inherent improvement in electron transport properties in the InAs/AlSb HEMT as opposed those of the GaAs or InP-based HEMT are illustrated in the compiled Hall data in Figure 1.3 [19]. The typical InAs/AlSb HEMT targets a sheet charge density of 3-4 $\times 10^{12}$ cm^{-2}, and exhibits a room temperature mobility of about 18,000 cm^2/Vs, as compared with 6,000 and 10,000 cm^2/Vs for quality GaAs and InP-based HEMTs, respectively.

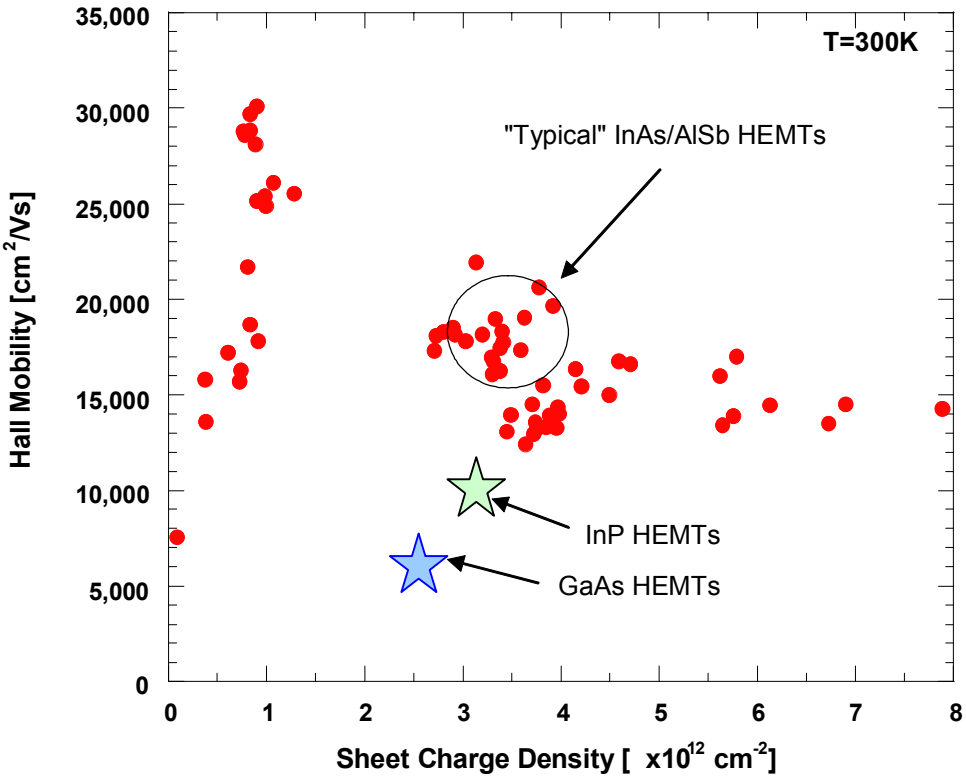


Figure 1.3 Compiled Hall data for various InAs/AlSb metamorphic HEMTs grown on GaAs substrates.

1.3. The Integration of InAs QW Electronic Devices into Circuits

The primary challenge inherent to the realization of integrated circuits that incorporate InAs QW-based active devices is the lack of a lattice-matched semi-insulating substrate. A semi-insulating substrate is essential in order to avoid substrate loss and parasitic coupling in high-speed circuits. InAs, on account of its narrow bandgap of 0.36 eV, cannot be made semi-insulating at room temperature. As shown in Figure 1.4, the only other semiconductors in the 6.1 Å group are GaSb and AlSb, neither of which is suitable as a substrates for epitaxially grown InAs-based devices. GaSb (0.6% mismatch) is always conductive at room temperature due to its relatively narrow

bandgap of 0.73 eV and the presence of a native defect, likely a doubly-ionized Ga-antisite, which renders undoped GaSb p-type with hole concentrations of approximately 10^{17} cm^{-3}. AlSb (1.2% mismatch) is very unstable in air, oxidizing rapidly (see Chapter 6 for an example), and therefore cannot be used as a substrate material.

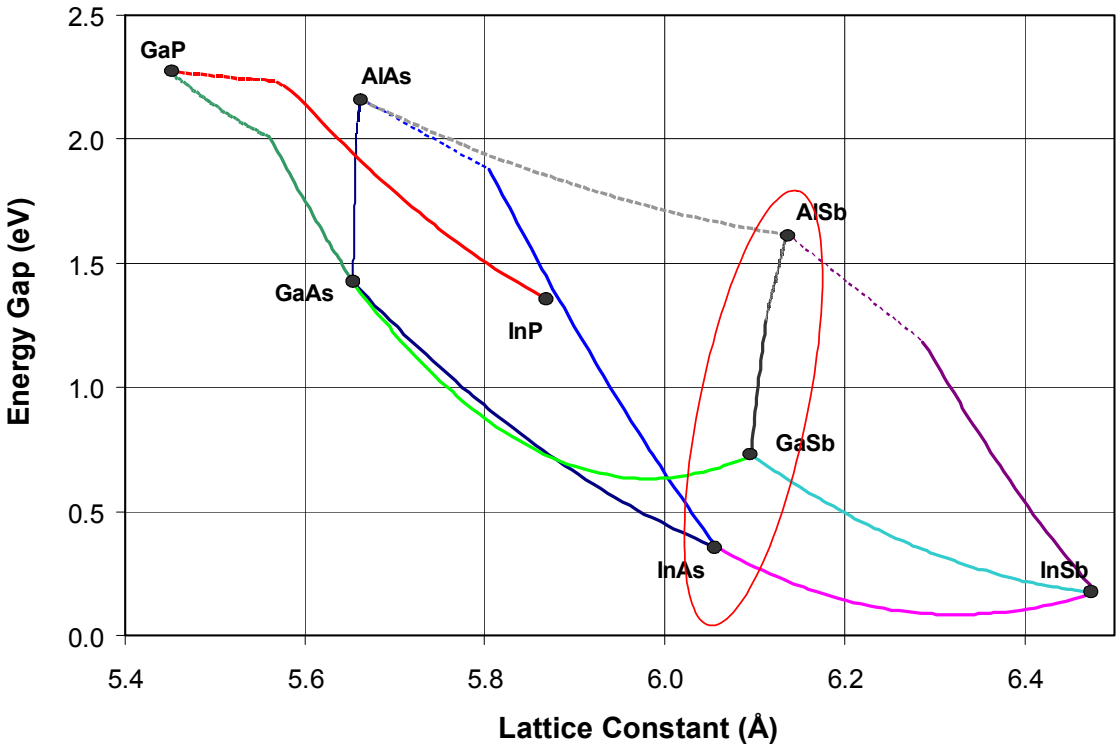


Figure 1.4 The III-V semiconductors (excluding the nitrides).

The absence of a lattice-matched substrate necessitates the development of novel integration methods for InAs-based electronics with semi-insulating substrates. In the case of the InAs quantum well RTD, there is an additional need to integrate the RTD with transistors in order to realize practical circuits. The specific approaches for integrated circuit fabrication can be divided into two general categories: (1) monolithic integration

and (2) hybrid integration, both of which can be applied to either the InAs subwell RTD or the InAs/AlSb HEMT. The monolithic integration technique vertically integrates the InAs-based device layers to the substrate (and possibly other active device layers) through stacked epitaxial growth. In contrast, hybrid integration grows and fabricates the InAs-based electronic devices independently, and subsequently integrates the device to a host substrate through the use of a substrate removal and transfer process. The two integration techniques are illustrated schematically in Figure 1.5 for the cases of both the RTD and the InAs/AlSb HEMT.

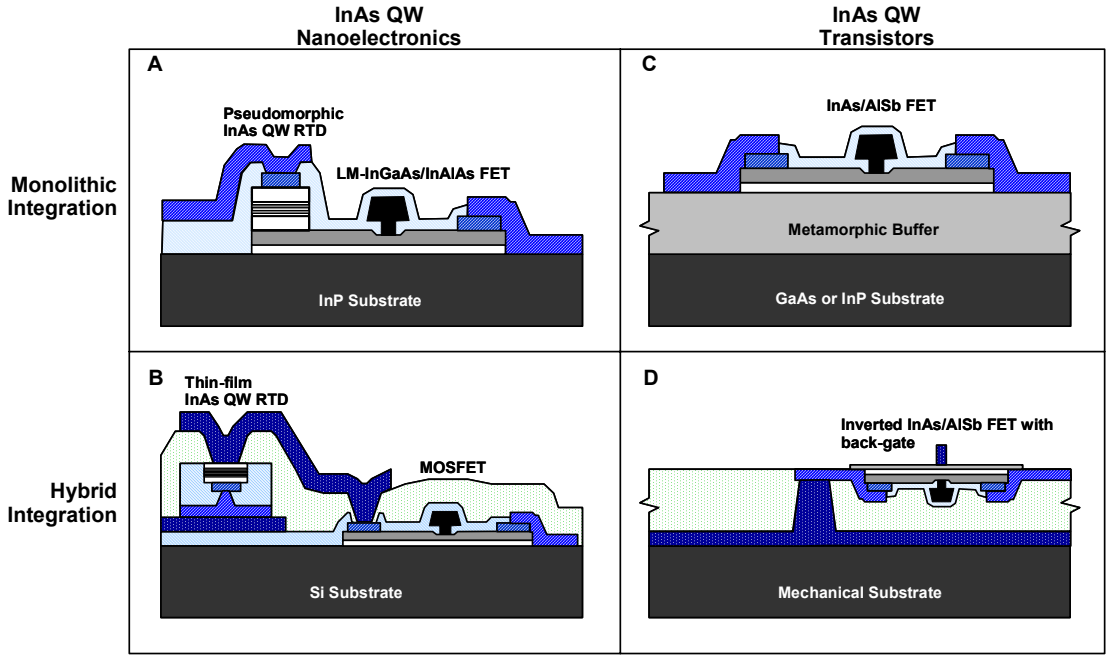


Figure 1.5 Methods of fabricating InAs QW electronic circuits.

1.3.1. Monolithic integration of pseudomorphic InAs subwell RTDs with InP-based Transistors (Figure 1.5(a))

Because the width of the InAs subwell in an InAs/$In_{0.53}Ga_{0.47}As$/AlAs RTD does not typically need to be larger than its elastically strained limit of about 30 Å on InP, the InAs/$In_{0.53}Ga_{0.47}As$/AlAs RTD can be safely grown on semi-insulating InP substrates. On account of the high etch selectivity that can be obtained between InP and the arsenides, thin 30 Å InP layers can serve as reliable etch stop layers separating vertically stacked $In_{0.53}Ga_{0.47}As$/ $In_{0.52}Al_{0.48}As$ HEMTs and InAs/$In_{0.53}Ga_{0.47}As$/AlAs RTDs. Since the integration of RTD and transistor is accomplished entirely through MBE growth, conventional InP semiconductor processing techniques can be employed in the integrated circuit fabrication. For this reason, the monolithic approach has been developed to a far greater extent than the hybrid approach. Using this method novel RTD-HEMT and RTD-HBT based digital logic [20], [21], memory cells [22]-[24], and analog-to-digital converters [25], [26], have been demonstrated.

1.3.2. Hybrid integration of RTDs with silicon integrated circuits (Figure 1.5(b))

The hybrid approach to integration of mixed material devices allows for the independent optimization of each technology on its preferred substrate in the most mature fabrication process. This approach has been most successfully applied in the fabrication of high-performance infrared (IR) focal plane array (FPA) imagers, in which an FPA of infrared photodiodes is attached to a CMOS-based readout integrated circuit (ROIC) by a type of flip-chip bonding. The electrical contacts and mechanical support are provided by indium solder bonds which are patterned on the pre-fabricated FPA chip. However, the alignment and die attachment of the IRFPA chip to the ROIC is capital intensive, as it

is performed by very expensive machinery, and is generally used on low-volume, high-cost parts. Using this method, hybrid infrared cameras using 2048 × 2048 pixel HgCdTe or InSb FPAs on CMOS ROICs have been fabricated [27]-[29].

In the case of InAs subwell RTDs to be integrated in this work, the FPA-style bonding method was infeasible due to the lack of availability of the bonding equipment, and due to the small scale of the circuits to be developed. Instead, the hybridization method used more closely resembles the schematic of Figure 1.5(b), which uses a process better suited to the financial and capital resources available. In this technique, the InP substrate is removed, and the thin-film RTD is bonded to the silicon integrated circuit using an alignable substrate transfer process [30]. This hybrid thin-film integration process has been previously demonstrated with InP-based photodiodes [31], [32], but has never previously been attempted with a resonant tunneling diode. The drawbacks of the thin-film hybridization method include the difficulty of reliably transferring the thin-film device and limitations on the minimum transferable device size and maximum device array size.

1.3.3. Monolithic metamorphic InAs/AlSb HEMTs (Figure 1.5(c))

Researchers have made significant progress on metamorphic growth of InAs/AlSb HEMTs on relaxed (Ga)AlSb buffers that accommodate the lattice mismatch of 7.2% between the GaAs substrate and InAs [5], [18]. After approximately 2 μm of the (Ga)AlSb buffer is grown, the threading dislocation defect densities are lowered from an initial density of approximately 10^{10} cm^{-2} to approximately 10^{8} cm^{-2}, which does not severely degrade the electron transport qualities of the InAs/AlSb 2DEG. The major drawback to this approach is the uncertain effect of the high dislocation density on the

gate leakage current and overall reliability of the HEMT relative to a defect-free HEMT. Nevertheless, all reported InAs/AlSb heterostructure transistors have been realized by metamorphic MBE growth on semi-insulating GaAs or InP substrates.

1.3.4. Hybrid transferred-substrate dual-gated InAs/AlSb HEMTs (Figure 1.5(d))

The transferred-substrate (TS) fabrication method allows the InAs/AlSb HEMT to be grown on a lattice-matched GaSb or InAs substrate, eliminating the high density of threading dislocations present in a metamorphic HEMT and allowing the HEMT material to reach its intrinsic limits. The HEMT is fabricated on the lattice-matched growth substrate, followed by the completion of on-chip passive devices such as interconnects, capacitors, and resistors. A low-K polymer such as benzocyclobutene (BCB) is spun and cured to a thickness of less than 20 μm. After vias are patterned and metal vias are patterned through the dielectric and a top side ground plane is metallized. The wafer is then inverted and bonded to a mechanical host substrate, after which the growth substrate (in this case GaSb or InAs) is selectively removed. The embedded transmission lines eliminate the need for a semi-insulating substrate, and provide a high impedance, low loss interconnect environment.

The TS fabrication method also allows for a more advanced transistor to be fabricated by allowing the back side of the active device to be accessed. This method was used to great success by Rodwell's group at UCSB in the fabrication of TS InP-based HBTs with laterally scaled collectors [33]. The reduction in the base access resistance and base-collector capacitance made possible in the TS-HBT resulted in devices with maximum oscillation frequencies over 800 GHz [34]. In the context of the InAs/AlSb HEMT, the TS approach allows for a second gate to be used on the other side

of the channel. This TS-HEMT could be realized as dual-gate HEMT for even higher speed operation, or as a back-gated HEMT in which the breakdown voltage is increased by the back gate's collection of impact-generated holes. These potential advantages of the TS InAs/AlSb HEMT are offset by difficulty of aligning a submicron back gate to the front side gate as well as the risk of damaging the device layers due to the very thin layers separating between the back gate and the InAs channel.

1.4. Organization of the Dissertation

The dissertation is organized by the specific type of integration method being used, starting with the hybrid integration of InAs subwell RTDs to CMOS integrated circuits, progressing to a monolithic InP-based tunnel diode-HEMT technology, and concluding with the metamorphic InAs/AlSb HEMT. While the transferred-substrate HEMT may allow the performance of the InAs/AlSb HEMT to achieve its fundamental limits, the development of the TS-HEMT is left for the future when the monolithic InAs/AlSb HEMT has been more thoroughly developed and is ready for the transition into the TS technology. Throughout, the dissertation is focused on integrated circuit compatibility, rather than simply optimization of the discrete InAs QW active device.

Chapter 2 covers the design of integrated RTD-CMOS circuits, starting with a description of the modifications made to the InAs/$In_{0.53}Ga_{0.47}As$/AlAs RTD epitaxial design in order to make it more compatible with CMOS circuitry, and continuing with a summary of the RTD-CMOS designs considered for hybrid thin-film integration. In Chapter 3, the development and implementation of the thin-film integration process that yielded the first ever RTD-CMOS integrated circuits are described. The improvement of

the RTD-CMOS hybrid integration process by lowering the parasitic capacitances associated with integration is presented in Chapter 4. Chapter 5 covers the design and characterization of monolithic microwave integrated circuits (MMICs) in the QMMIC technology in which InP-based tunnel diodes are monolithically integrated with $In_{0.53}Ga_{0.47}As$/ $In_{0.52}Al_{0.48}As$ HEMTs. Chapter 6 introduces the metamorphic InAs/AlSb HEMT in the context of integrated circuit development, describing the HEMT process development and the novel DC device characteristics. Finally, Chapter 7 details the remarkable RF small-signal and noise characteristics of the MMIC-compatible InAs/AlSb HEMT.

The unique contributions of this work include the following:

1. The first ever RTD-CMOS circuits were demonstrated using the baseline thin-film integration method described in Chapter 3. The process for the integration of planarized thin-film InP-based devices can be extended to virtually any two terminal compound semiconductor device.

2. The analysis of the components of the parasitic capacitance in the thin-film integration process establishes the limiting factors in determining the speed of thin-film integrated devices, helps to identify the inherent tradeoffs, and suggests process modifications needed to achieve the desired performance.

3. The InAs/AlSb MMIC fabrication technology was developed which yielded InAs/AlSb HEMTs with best-to-date speed, power, and low-noise performance in this material system, in addition to the first InAs/AlSb integrated circuits.

4. A comprehensive characterization of the RF noise properties of the InAs/AlSb HEMT gives an unprecedented understanding RF noise performance and the influence of

impact ionization on the RF noise characteristics. This characterization and subsequent analysis is valuable in the design of InAs/AlSb HEMT-based low-noise amplifiers and suggests how to target the selection HEMT structure and DC bias conditions for minimum noise as at a given frequency.

CHAPTER 2

RTD-CMOS DESIGN

2.1. RTD Device Design for Integration with CMOS: RTDs with $In_{0.52}Al_{0.48}As$-AlAs Composite Barriers

The initial prefabricated RTDs have an area ranging from 4×4 μm^2 to 16×16 μm^2. To match the RTDs to the CMOS circuit requirements, a peak current density range of several orders of magnitude must be available, since scaling the diode area is constrained. To accomplish this, the quantum barrier thickness was increased, thereby lowering the peak current density. Because the AlAs barrier is strained, its thickness is limited to approximately ten monolayers, or 28 Å in thickness. For this reason, a lattice-matched $In_{0.52}Al_{0.48}As$ pre-barrier was used to realize further lower peak current density, at the expense of PVCR. The overall device structure is shown in Figure 2.1(a), with the corresponding conduction band profile for an RTD with 25 Å $In_{0.52}Al_{0.48}As$ pre-barriers plotted in Figure 2.1(b). If it is assumed that the only significant transmission at the peak occurs in the energy band between $(E_1 - \Gamma_1/2)$ and $(E_1 + \Gamma_1/2)$, where E_1 and Γ_1 are the resonance energy and full-width half-maximum (FWHM) of the transmission, then the peak current density will be proportional to Γ_1. In theory, Γ_1 should then have an exponential dependence on barrier thickness, and can be approximated as

$$\Gamma_1 \cong \frac{1}{2\pi} E_1 \exp(-2\beta L_B), \tag{2.1}$$

where L_B is the barrier thickness and $\beta = \sqrt{2m_e^*(V_o - E_1)}/\hbar$, with m_e^* as the electron effective mass and V_o as the barrier energy height.

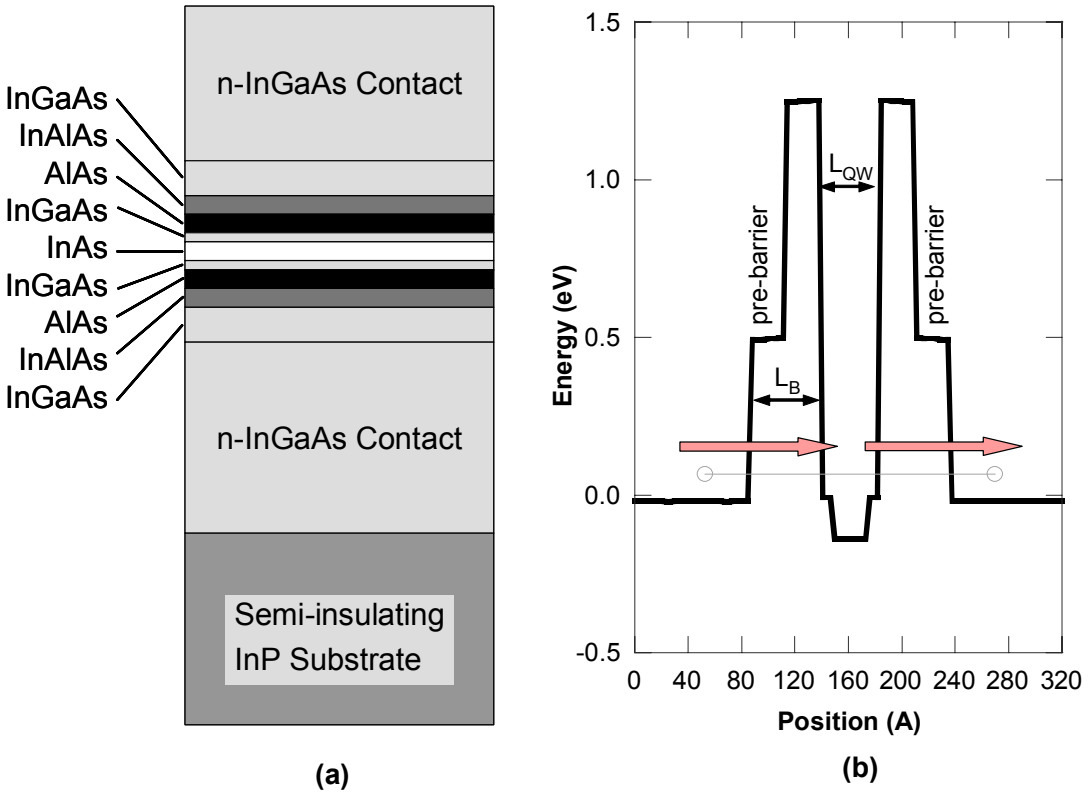


Figure 2.1 (a) Schematic of the complete RTD layer structure with composite $In_{0.52}Al_{0.48}As$/AlAs barriers. (b) Corresponding conduction band profile with the first resonance.

Figure 2.2(a) shows the calculated FWHM resonance width for the same RTD structure shown in Table 1.2 with $In_{0.52}Al_{0.48}As$ pre-barriers of thickness varying from zero to 32 Å. The results show a perfect exponential dependence of Γ_1 vs. pre-barrier thickness with a sensitivity of −0.078 decade/Å. An experimental plot of the peak currents as a function of the InAlAs pre-barrier thickness is shown in Figure 2.2(b) [35]. The only intentional variation within each set is the pre-barrier thickness. The two sets represent two different quantum well thicknesses, with L_{QW} = 40 Å and L_{QW} = 50 Å. The available peak current densities span four orders of magnitude and follow an exponential dependence on the pre-barrier thickness as expected from theory. The sensitivity of J_p to the pre-barrier thickness also agrees well with that of the simulated the FWHM resonance

width, showing a sensitivity of −0.070 decade/Å for an RTD with L_{QW} of 40 Å and −0.083 decade/Å for an RTD with L_{QW} of 50 Å.

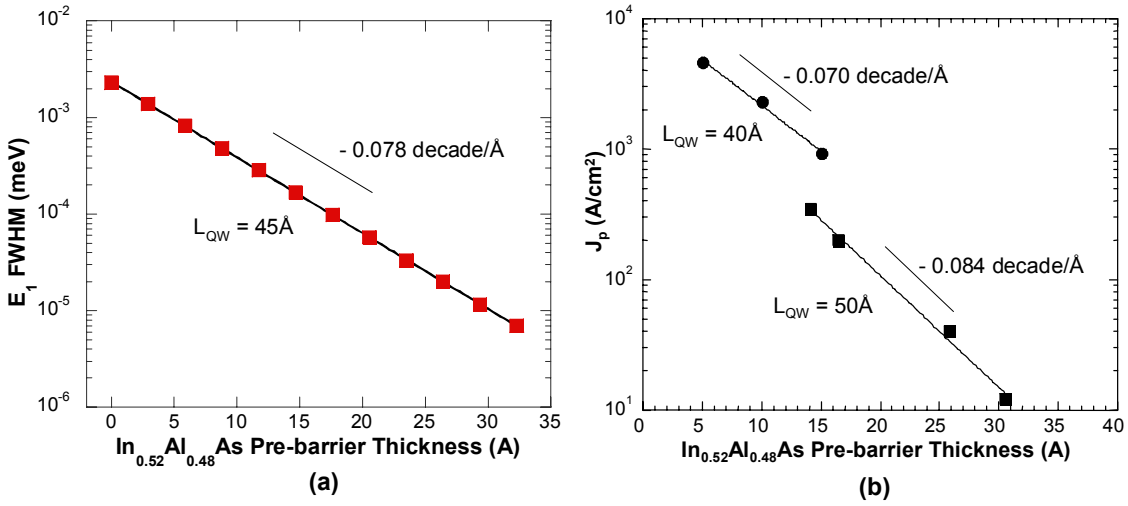


Figure 2.2 (a) Simulated FWHM linewidth of the first resonance in an InAs/$In_{0.53}Ga_{0.47}As$/AlAs/$In_{0.52}Al_{0.48}As$ RTD. (b) Experimental dependence of the RTD peak current density on the $In_{0.52}Al_{0.48}As$ pre-barrier thickness.

2.2. RTD-CMOS Circuit Designs Proposed For Thin-Film Integration

The first task in developing hybrid RTD-CMOS circuits was the identification of particular circuits where the availability of the RTD would make a significant improvement in overall circuit speed, power consumption, or density. To meet this goal, a variety of digital and mixed signal circuits were designed and simulated using HSPICE. The circuits were limited to low levels of integration, with no more than two RTDs or about twenty MOSFETs, to improve the possibility of success given the challenges and uncertainties probable in the RTD-CMOS thin-film integration process. There were three general classes of circuits studied: (1) comparators and quantizers, (2) RTD-based

memory cells, and (3) digital logic gates. Details of the designs are beyond the scope of this work, but are available in [36].

While detailed BSIM3 models for the MOSFETs were available from the MOSIS foundry for use in circuit design, no proven circuit model exists suitable for the RTD. The RTD model used for design is a physics-based model, developed at Texas Instruments, Inc. by Tom Broekaert that uses equation-governed nonlinear voltage-controlled current sources to model the RTD current-voltage characteristic. The derivation of the static J-V equations [37] is similar to those used in previous physics-based RTD models, in which the form of resonant tunneling current density is determined analytically using the effective mass approximation, with the integration simplified by the assumption that the resonance linewidth Γ_n is small relative to $k_B T$ [38]. Fitting parameters are applied to the J-V equations to yield better agreement with measured RTD I-V characteristics. The details of the RTD model have been reported previously [39], and will not be addressed further here, except to note that a static parallel capacitance with a fixed value ranging from 2–4 fF/μm^2 (dependent on device structure) was used in place of the prescribed voltage dependent capacitance. This modification was necessary to improve the model's numerical stability in HSPICE.

2.2.1. Fundamental RTD-CMOS building blocks

There are two fundamental RTD-nMOSFET configurations considered in the designs, which will be referred to as the drain-loaded MOSFET and gate-loaded MOSFET. The drain-loaded MOSFET is an nMOSFET with an RTD integrated at the drain terminal, while the gate-loaded MOSFET is an identical nMOSFET with the RTD connected at the gate, as shown in Figure 2.3. The drain-loaded RTD/MOSFET should

function as a Schmitt-inverter, with the RTD switching abruptly from low to high (output high to low) voltage when the current pulled by the nMOSFET is increased (by increasing V_G) beyond the peak current I_p. Likewise, when the voltage is lowered (V_G decreased to just above threshold), the RTD switches back to the lower voltage. The gate-loaded RTD/MOSFET circuit functions as a threshold current comparator with the output switching abruptly when the when the current through the RTD is increased above threshold (I_p). The current gain is dictated by the noise margin of the input current to the RTD.

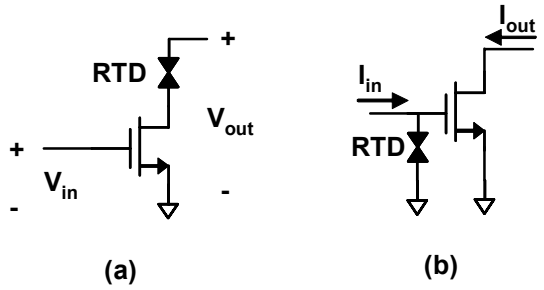


Figure 2.3 (a) Circuit schematic of the drain-loaded RTD-nMOSFET. (b) Circuit schematic of gate-loaded RTD-nMOSFET.

2.2.2. RTD-CMOS comparators and quantizers

The RTD's fast switching through the negative differential resistance region, along with its self-latching characteristics make it ideally suited to comparators, where the circuit switches and holds when an input threshold is exceeded. Not only is improved speed possible, but also greatly reduced component count due to the elimination of the need for positive feedback circuitry.

Figure 3.4 shows a schematic for a simple RTD/CMOS current mode comparator designed by Y. Joo. A reset clock is required to select the lower stable state during a transition of input current from high to low. The output voltage switches when the input current is same as peak current of the RTD. In this circuit two current mirrors are designed to support peak current (I_p) and input current (I_{in}) to provide for robustness. An external reset signal is necessary to reset the voltage across the RTD below its peak current voltage (V_P) before the decision.

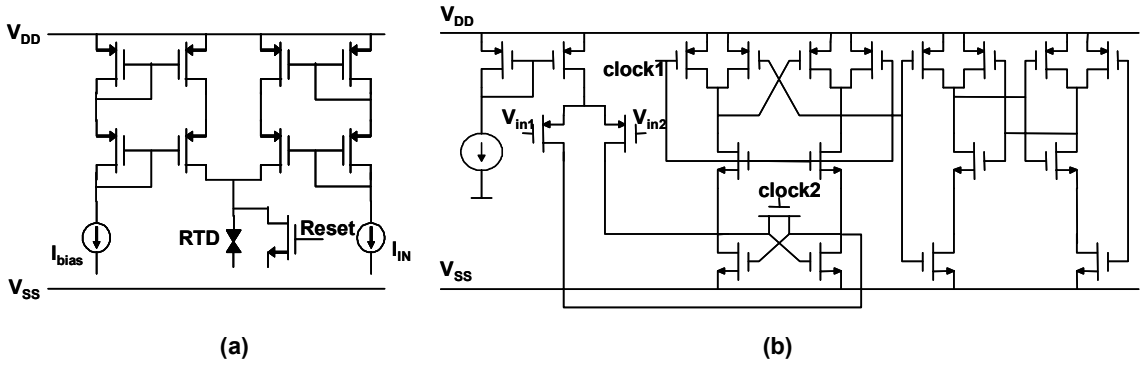


Figure 2.4 (a) Circuit schematic of the RTD-CMOS current mode comparator. (b) Circuit schematic of an all-CMOS comparator.

Simulation results of the designed comparator in 0.8-micron CMOS assuming minimal RTD and integration parasitics are provided below in Table 2.1, a showing a 60% improvement in power dissipation with a factor of two reduction in component count. Note that the component count could be reduced from 10 to 6 in the RTD-CMOS design if single-cascode current mirrors were substituted for the double-cascode mirrors in the design shown.

Table 2.1 Simulated performance of RTD-CMOS and CMOS-only comparators

	RTD-CMOS I_p = 80 µA	RTD-CMOS I_p = 400 µA	CMOS
Maximum Speed (Mbps)	200	800	800
Power Consumption (mW)	0.24	2.4	5.6
Device Count	10 (6 with single-cascode current mirrors)		21

The self-resetting current comparator circuit shown in Figure 2.5 was designed by J. Chang [36]. By using two RTDs, this circuit eliminates the undesirable requirement of an external reset signal. This circuit incorporates rising edge detectors to allow for self resetting operation of the RTDs. This circuit uses three different bias lines, two for RTDs and one for the rising edge detector circuit. This design should be used with RTDs with very low currents in order to lower power consumption. For example, by using an RTD with peak current of 4 µA the power consumption of this circuit reduces to 40 µW. This design also provides a very high transimpedance gain of hundreds of megaohms.

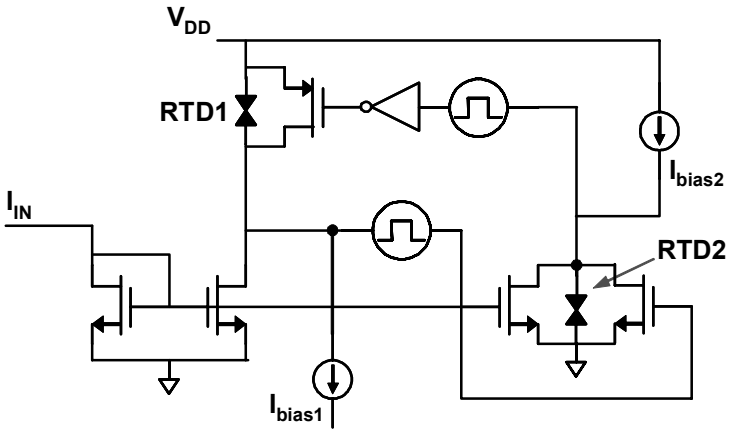


Figure 2.5 Schematic of the RTD-CMOS self-resetting current comparator.

2.2.3. RTD-CMOS memory designs

The bistable latched RTD pair had been proposed as a memory cell as early as 1960 by Goto [40]. The "Goto-latch" is not useful for large-scale memory applications because the state of the latched pair must be sensed directly which requires large RTD restoring currents. This translates into large peak current densities over 10^4 A/cm^2 and because the PVCR is limited, large valley currents and standby power result [39].

The tunneling SRAM (TSRAM), proposed by J. P. A. van der Wagt [41], is a dynamically sensed RAM cell that uses a latched RTD pair as a charge keeper, so that the 1-transistor memory cell does not need to be refreshed. The concept of the RTD binary TSRAM cell is illustrated in Figure 2.6, where the RTD-MOS TSRAM is seen as evolving from the classic 1-transistor MOS DRAM (Figure 2.6(a)), with the RTD pair added to hold the charge stored in the MOS capacitor (Figure 2.6(b)). Ideally, the storage capacitor is replaced by the intrinsic device capacitance of the RTD pair charge keeper, shown in Figure 2.6(c). A sense amplifier detects the voltage shift caused by charge sharing between the storage capacitor and the bit line, as in a conventional 1-T MOS memory array. If an integrable silicon tunnel diode is developed, significant power savings can be realized by eliminating the power dissipated during the refresh cycle, which can be significant. The figures of merit for the RTDs in the TSRAM cell differ from those used for switching in that while high PVCR is still preferred, the speed index is not important. The RTD currents can be very low (sub-pA) since they need only counteract the leakage and off-state currents through the transistor.

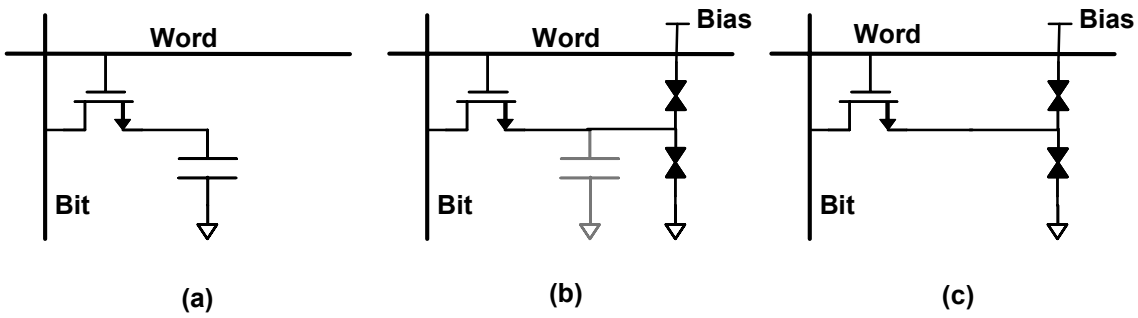


Figure 2.6 The evolution of the tunneling SRAM (TSRAM).

The silicon-based TSRAM is useful where there the leakage currents are higher than those of a normal DRAM transistor. This may occur when large, dense on-chip memory is needed in a conventional digital CMOS process. Since refresh rates are proportional to the worst-case transistor leakage current, an improvement in standby power can be realized with the TSRAM. Also, the TSRAM illustrates how any high-speed dynamic CMOS logic circuit can be converted into a static circuit by using the very low current density latched RTD pair at the storage node.

A multistate SRAM was also designed which used a multiple-peak RTD (several RTD's stacked in series) as a load for an nMOSFET current source. For an *N*-peak RTD, there will be (*N*+1) stable states. A nine-state memory was demonstrated by monolithically integrating a multiple-peak RTD with HEMTs on InP using an analogous design [42] While the multistate SRAM offers a great improvement in functional density, its performance is limited by the need to charge and discharge the RTD capacitance through the relatively large series resistance in the RTD stack. The worst case charging time resulting from this series RC ladder precludes the possibility of useful multistate SRAM cells with low static power consumption, and the multistate SRAM design was not pursued.

2.2.4. RTD-CMOS digital logic

A variety of novel digital logic families have been proposed that use the RTD's folding I-V characteristic, fast switching speed, and bistability to achieve an improvement in speed, power consumption, or circuit density [43]-[47]. A static RTD-CMOS (RTD-nMOS) gate consists of an RTD pull-up load and a pulldown network of n-transistors that determines the logic operation performed by the gate. A generic static QMOS logic gate is illustrated in Figure 2.7(a). Figure 2.7(b) shows the load lines of this static QMOS logic gate. The principle of operation of a static QMOS gate is as follows. When the inputs, $I_1, I_2, \ldots, I_m$, of the static QMOS gate are such that the pulldown network is turned off, there is no current flow through the circuit and hence the voltage at node out equals the supply voltage, i.e. logic high.

The transistors in the pulldown network are so designed that when the inputs $I_1, I_2, \ldots, I_m$, of the static QMOS gate are such that the pulldown network is turned on, the current through the circuit exceeds the peak current of the RTD. This causes the RTD operating point to jump to PDR2 resulting in the output voltage at node out going low, corresponding to a logic low.

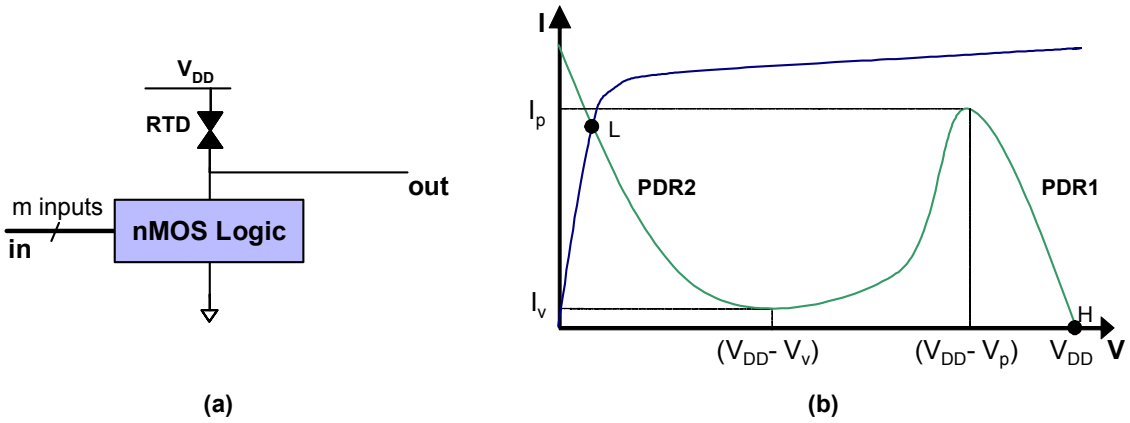


Figure 2.7 (a) Schematic of a static RTD-nMOS logic gate. (b) Load lines for static RTD-nMOSFET gate operating point.

A binary logic circuit is said to operate in bistable mode when its output is latched, and any change in the input is reflected in the output only when a clock or other evaluation signal is applied. The chief disadvantage of these circuits is the requirement of an AC power source whose frequency determines the maximum switching frequency. The RTD-nMOS logic circuits described below use a DC power supply and multiphase clocks but the clock signals are not required to supply large amounts of power as in the case of the earlier circuits. The operating principle of the new bistable element may be understood by considering the simplified circuit shown in Figure 2.8(a). The RTD forms the active load in the circuit. There are *m* inputs in the n-logic block which determines the circuit function, one clock transistor which controls the evaluation of the gate, and a bias transistor that maintains quiescent current through the RTD while also controlling the precharging of the gate output. Figure 2.8(b) shows the load lines for the bistable logic gate. Switching of the bias transistor is used to reset the state of the gate or to maintain a quiescent current through the RTD which is between its peak and valley currents. The clock transistor is designed such that if the n-block is turned on, turning the clock

transistor on will cause the current through the RTD to exceed its peak current value thus switching the state of the gate. This logic family does, however, consume significant standby power, due to the requirement that the RTD be biased with a quiescent current greater than the RTD's valley current. This becomes less of a limitation when the gate is run at high clock frequencies, and dynamic power consumption dominates the overall power dissipation.

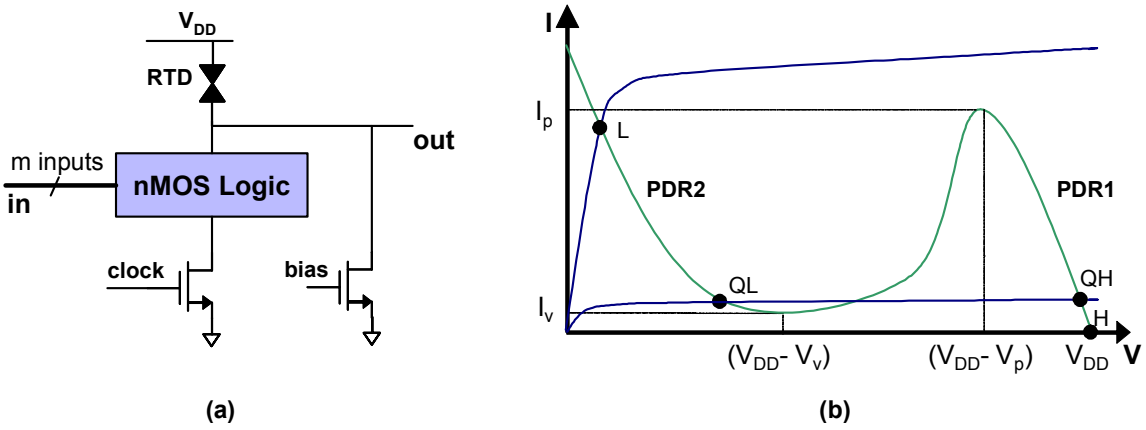


Figure 2.8 (a) Schematic of a bistable RTD-nMOS logic gate. (b) Load lines for bistable RTD-nMOSFET gate operating point.

2.2.5. Evaluations of RTD-CMOS designs

From the initial studies, it appears unlikely that the RTD-CMOS digital logic designs would result in dramatic speed improvement relative to the best dynamic CMOS logic designs. Such improvements in speed and power consumption are possible, however, in analog and mixed signal applications, particularly analog-to-digital conversion (ADC). For this reason, the comparator designs were the primary focus of the hybrid integration through thin-film bonding. In addition, the comparators had the

advantage of requiring only a single RTD in a circuit, which was advantageous due to the challenges of the thin-film hybrid integration. Although a method of thin-film integration for multiple RTDs to CMOS was eventually developed in this work, the circuit demonstrations were carried out using the conventional thin-film transfer method described in the following chapter.

CHAPTER 3

THE RTD-CMOS THIN-FILM INTEGRATION PROCESS: DEVELOPMENT AND DEMONSTRATIONS

3.1. Substrate Transfer of RTD Arrays

To gauge our ability to integrate RTDs to silicon, an experiment was undertaken whereby large arrays would be transferred and bonded to a silicon host substrate, without integrating the RTDs to bond pads on the host substrate. Similar experiments were conducted previously with discrete high PVCR InAs/$In_{0.53}Ga_{0.47}As$/AlAs RTDs bonded to host substrates. It was found that there was some non-uniform variation from device to device as well as a slight increase in series resistance after substrate transfer, although the PVCR did not change appreciably from its on-wafer value of approximately 30 [48]. The integration of a chip of parallel arrays of RTDs onto a silicon host substrate allows a closer investigation of the effects of epitaxial lift off (ELO) and substrate transfer on the yield of transferred substrate RTDs. Although a given single device's I-V characteristics may not be altered by the substrate transfer process, a large parallel array of small RTDs will show a measurable shift in current or decrease in PVCR if a fraction of them are destroyed or degraded in the process.

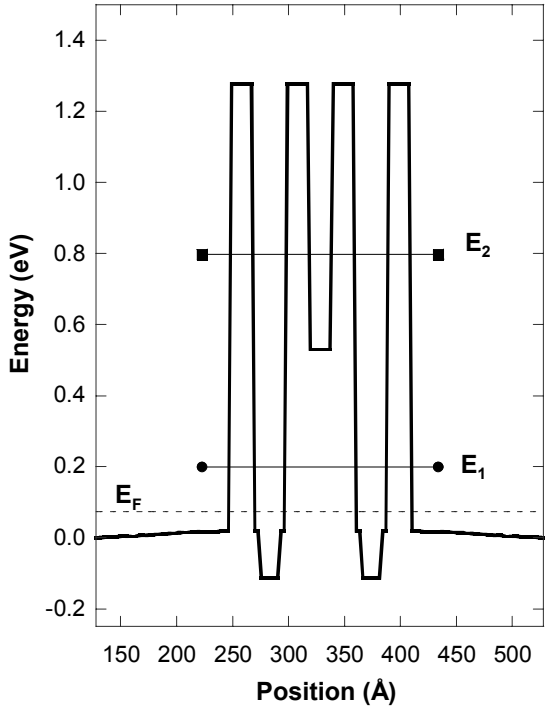
3.1.1. Experimental procedure

The epitaxial structure shown in Figure 3.1 was grown using solid source molecular beam epitaxy (MBE) on an n-InP substrate, at the Texas Instruments Dallas research facility. The RTD structure is a double-well structure separated by a 21Å

$In_{0.52}Al_{0.48}As$ barrier which was designed to offer a low peak current density on the order of the RTDs to be used to integrate to the CMOS circuits. Arrays of RTD contacts were defined with electron beam lithography with nominal sizes ranging from 0.2×0.2 μm to 1.0×1.0 μm, and Ti/Pt/Au contacts were e-beam evaporated and lifted off. The RTDs were mesa etched in H_2SO_4: H_2O_2: H_2O (1: 8: 160), using the contact as the etch mask. A partially planarizing spin-on glass (SOG) dielectric layer is spun and cured in addition to the 500–1000 Å PECVD Si_3N_4 that is normally used for passivation. The SOG is then etched back in a CF_4/O_2 plasma until the RTD contacts are exposed. An interconnect and bond pad layer is then patterned with conventional photolithography, and Ti/Au is lifted off. The set of RTDs in the each array were electrically linked with a Ti/Au contact over the SOG. In addition to studying the potential of integrating arrays, this investigation demonstrates the feasibility of using this SOG passivation and planarization process for future thin-film structures. For each device size, five different array sizes were incorporated onto the InP wafer: 1, 10, 100, 1000, and 10,000 RTDs. Complete I-V measurements were conducted before ELO and transfer.

	Composition	Thickness (Å)	Doping (cm^{-3})
17	$In_{0.53}Ga_{0.47}As$	600	1E19
16	$In_{0.53}Ga_{0.47}As$	200	1E18
15	$In_{0.53}Ga_{0.47}As$	50	
14	AlAs	20	
13	$In_{0.53}Ga_{0.47}As$	6	
12	InAs	18	
11	$In_{0.53}Ga_{0.47}As$	6	
10	AlAs	20	
9	$In_{0.52}Al_{0.48}As$	21	
8	AlAs	20	
7	$In_{0.53}Ga_{0.47}As$	6	
6	InAs	18	
5	$In_{0.53}Ga_{0.47}As$	6	
4	AlAs	20	
3	$In_{0.53}Ga_{0.47}As$	50	
2	$In_{0.53}Ga_{0.47}As$	200	1E18
1	$In_{0.53}Ga_{0.47}As$	2000	1E19
0	InP substrate		

(a)



(b)

Figure 3.1 (a) Epitaxial layer structure of the double quantum well InAs/$In_{0.53}Ga_{0.47}As$/AlAs RTD designed for low peak current density. (b) Corresponding conduction band profile with first and second resonances.

Figure 3.2 illustrates the basic steps for substrate removal and bonding to a host substrate. An Apiezon W black wax handling layer was applied before the substrate removal, and also serves to protect the devices from the wet chemical etching used for the InP substrate removal. The InP substrate was etched in an HCl: H_3PO_4 (3: 1) solution until the InP substrate was cleared (about two hours). After the InP substrate was removed, the devices and handling layer were briefly immersed in a weak oxide etch (NH_4OH:H_2O 1:15), then rinsed in de-ionized (DI) water. Because these RTD arrays require backside contacting, a Ti/Au contact is evaporated onto the back of the thin-film devices, contacting the n^+ $In_{0.53}Ga_{0.47}As$ layer closest to the InP substrate, even though the e-beam evaporation can cause the black wax to melt partially. The devices are

subsequently transferred and metal-metal bonded to a Ti/Au-plated silicon host substrate. The handling layer was dissolved in trichloroethylene (TCE). A final rapid thermal anneal for 30 seconds at 350 °C in a N_2 ambient served to bond the metal layers to provide good adhesion and electrical contact. Figure 3.3 shows a photomicrograph of the final transferred structure on silicon.

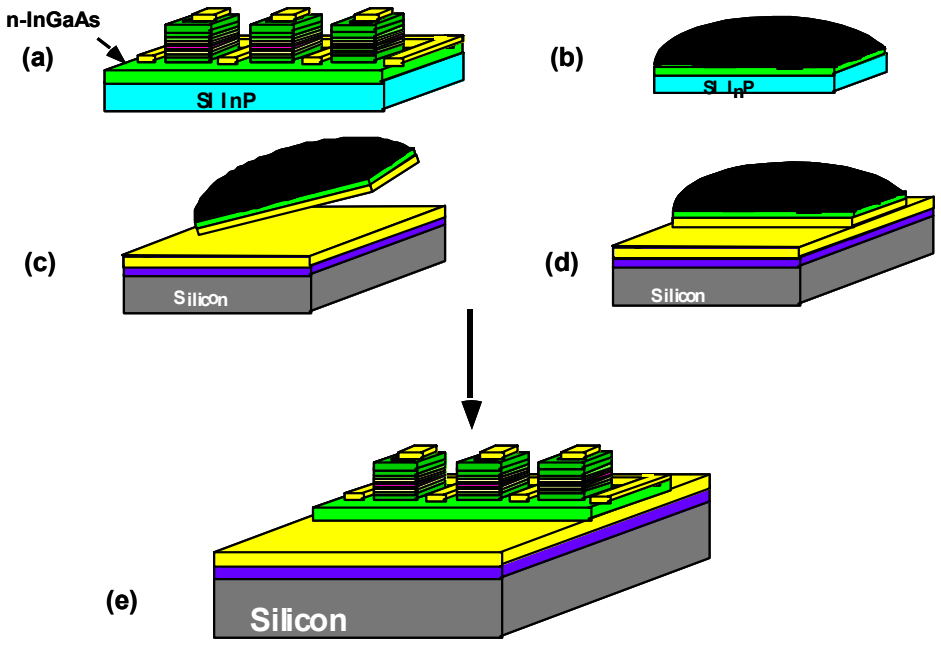


Figure 3.2 The epitaxial lift-off and substrate transfer process used for the transfer and bonding of the RTD arrays onto a silicon host substrate.

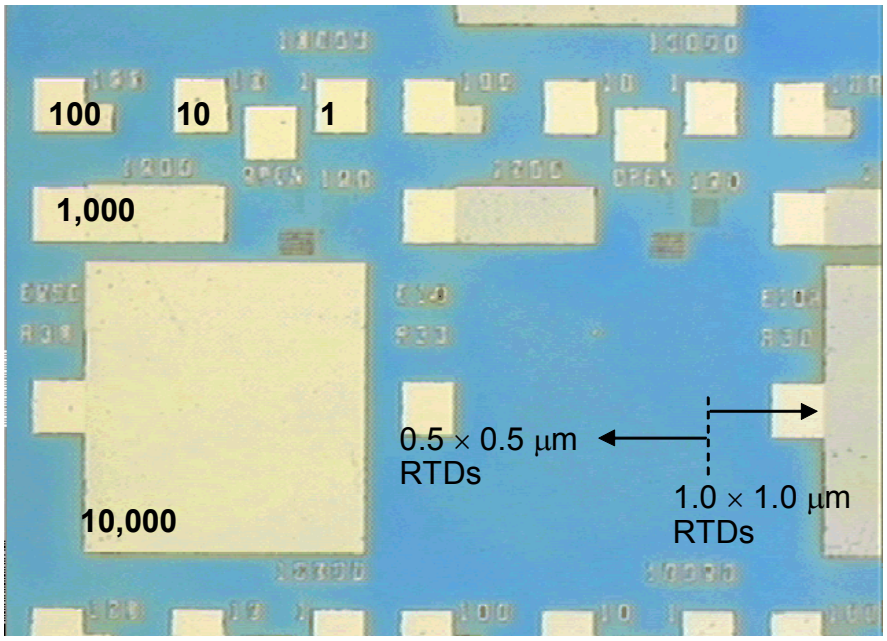


Figure 3.3 Photomicrograph of the InAs/$In_{0.53}Ga_{0.47}As$/AlAs RTD array chip bonded to silicon.

3.1.2. Results and discussion

The measured RTD I-V characteristics both before and after ELO showed a very slight difference between a forward voltage sweep and a reverse voltage sweep. (A forward sweep, in the current context, is defined as a sweep from negative to positive voltage, where the positive terminal is the top contact of the RTD and the negative terminal is the back (substrate) contact.) The peak current for a given array would usually be slightly lower for a forward sweep compared with the reverse voltage sweep, and the valley current was always 10-40% lower in a forward sweep, both on-wafer and after substrate transfer. Nevertheless, the difference between the same array before and after ELO is small, as can be seen in Figure 3.4 for both forward and reverse sweeps of arrays of 0.4 × 0.4 μm RTDs. Note that there was NDR only on the negative polarity, even though the RTD epilayers were nominally symmetric. This asymmetry was likely a

product of non-ideal interface formation in the MBE growth. In general, the lower the peak current density, the more severe is the asymmetry in the RTD I-V curve.

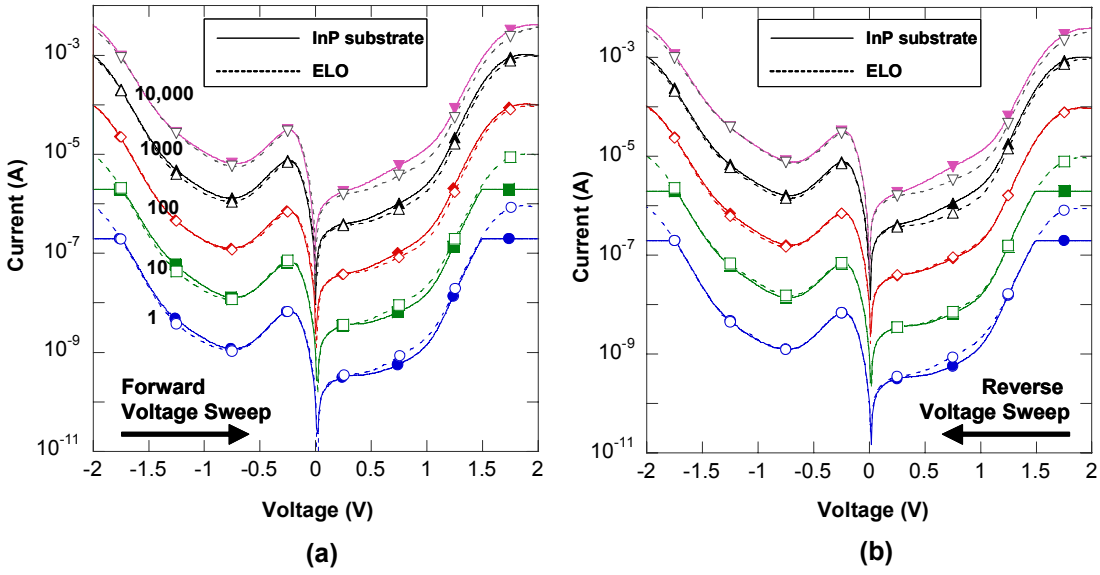


Figure 3.4 (a) Forward and (b) reverse I-V curves of arrays of parallel RTDs.

A measured I-V curve (reverse sweep) of a single 0.4×0.4 μm RTD before and after ELO is plotted on a linear scale in Figure 3.5(a) with the same curves for a 1,000 RTD array in Figure 3.5(b). Note that the RTD current does drop slightly (6.4%) for the 1,000 RTD parallel array, which could be an indication of the failure of a fraction of the devices in the array. The array's PVCR is not adversely affected by the ELO process, however.

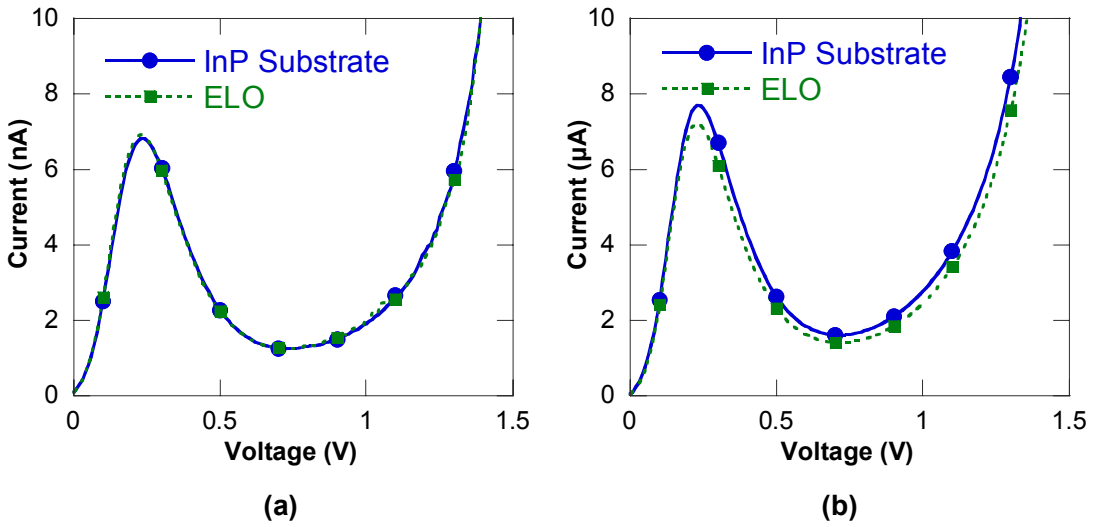


Figure 3.5 (a) Measured single RTD I-V curves on the InP substrate and after epitaxial lift-off. (b) Measured I-V curves for a 1,000 RTD array on the InP substrate and after ELO.

In order to gain a more complete understanding of the effect of substrate removal and bonding on the low current density RTDs, the measured DC device parameters are tabulated and plotted in Figure 3.6. These data do not show any clear trend indicating a consistent difference between the RTD arrays measured on-wafer and RTD arrays transferred to silicon, with the exception of a decrease in the valley current measured in the forward sweep and correlated enhancement of the PVCR. The plots of peak current vs. array size also do not support the assumption that a fraction of the RTDs in a large array are lost either by disconnecting from the array or by shorting between the terminals, since there is no decrease in the average peak current (Figure 3.6(c, d)) nor increase in average valley current (Figure 3.6(g, h)) of the RTD arrays. Also, no detectable change in the variation of the DC parameters from array to array due to ELO was observed. Finally, there is no indication of a change in series resistance as indicated by the lack of a

shift in the peak voltage (Figure 3.6(a, b)), although this effect is very dependent on the area of the back contact layer and particulars of bonding to the host substrate.

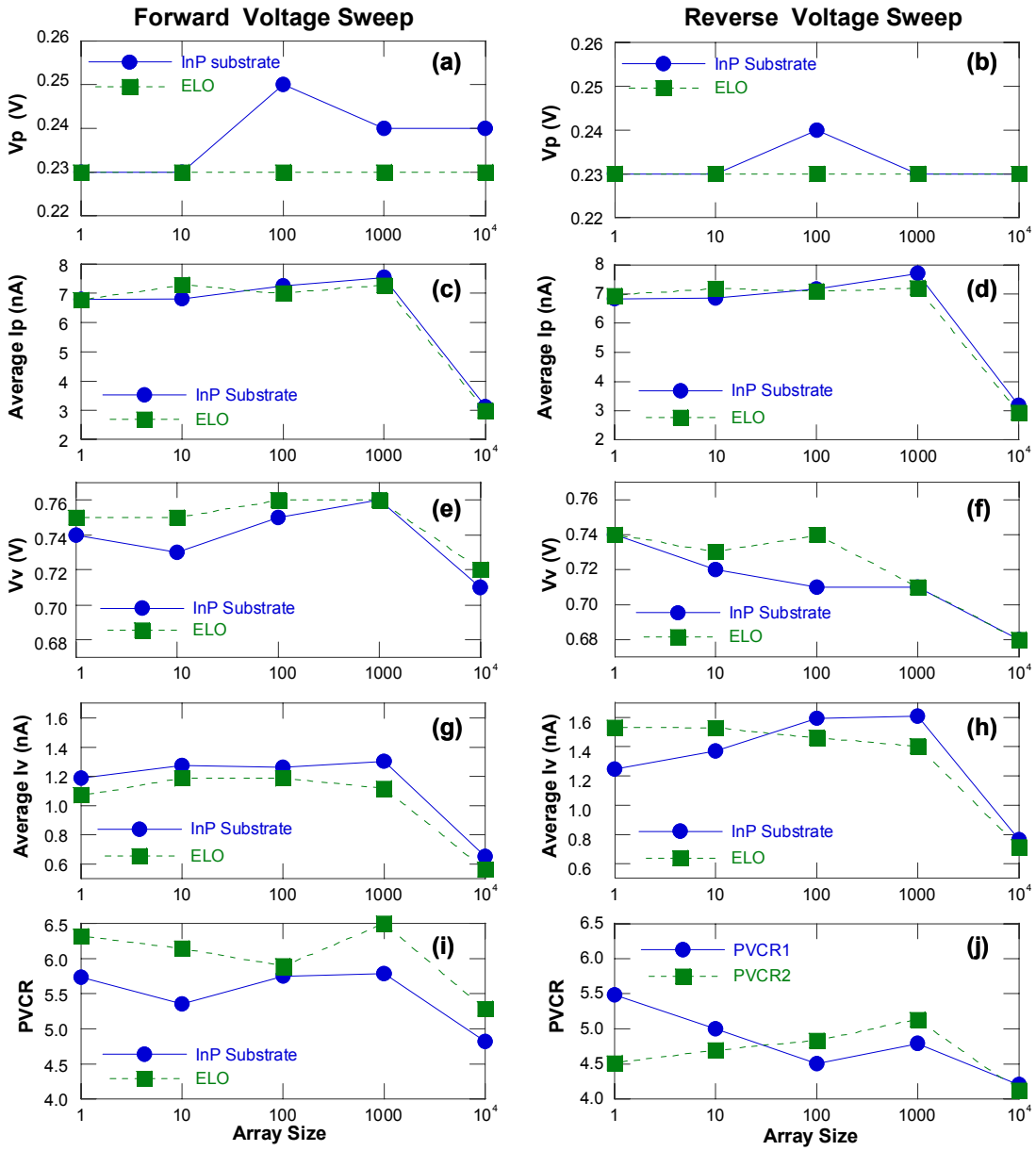


Figure 3.6 The measured DC parameters of the parallel RTD arrays are plotted for forward (left column) and reverse (right column) voltage sweeps.

3.2. The Thin-Film Integration Process

The ELO and host substrate bonding process described in the previous section and illustrated in Figure 3.2 do not allow the thin-film devices to be aligned precisely with respect to features on the host substrate. This makes integration to a CMOS chip impossible because the thin-film device must be accurately (± 10 μm) aligned to features on the host substrate. By bonding the thin-film devices to a transparent transfer diaphragm in the transfer process, the thin-film devices can be aligned with respect to features on the host substrate, with the versatility to pick and place individual devices [30]-[32], as illustrated schematically in Figure 3.7. First, the prefabricated InP devices are coated in a black wax handling, followed by substrate removal and bonding to a Mylar transfer diaphragm (Figure 3.7(a-c)). The black wax is then removed in TCE (Figure 3.7(d)). The devices are flipped, aligned to the bond pad on the host CMOS chip, then van der Waals bonded to the host chip with the application of slight pressure (Figure 3.7(e-g)). Figure 3.7(h) illustrates the finished thin-film integrated circuit after post-transfer processing is complete.

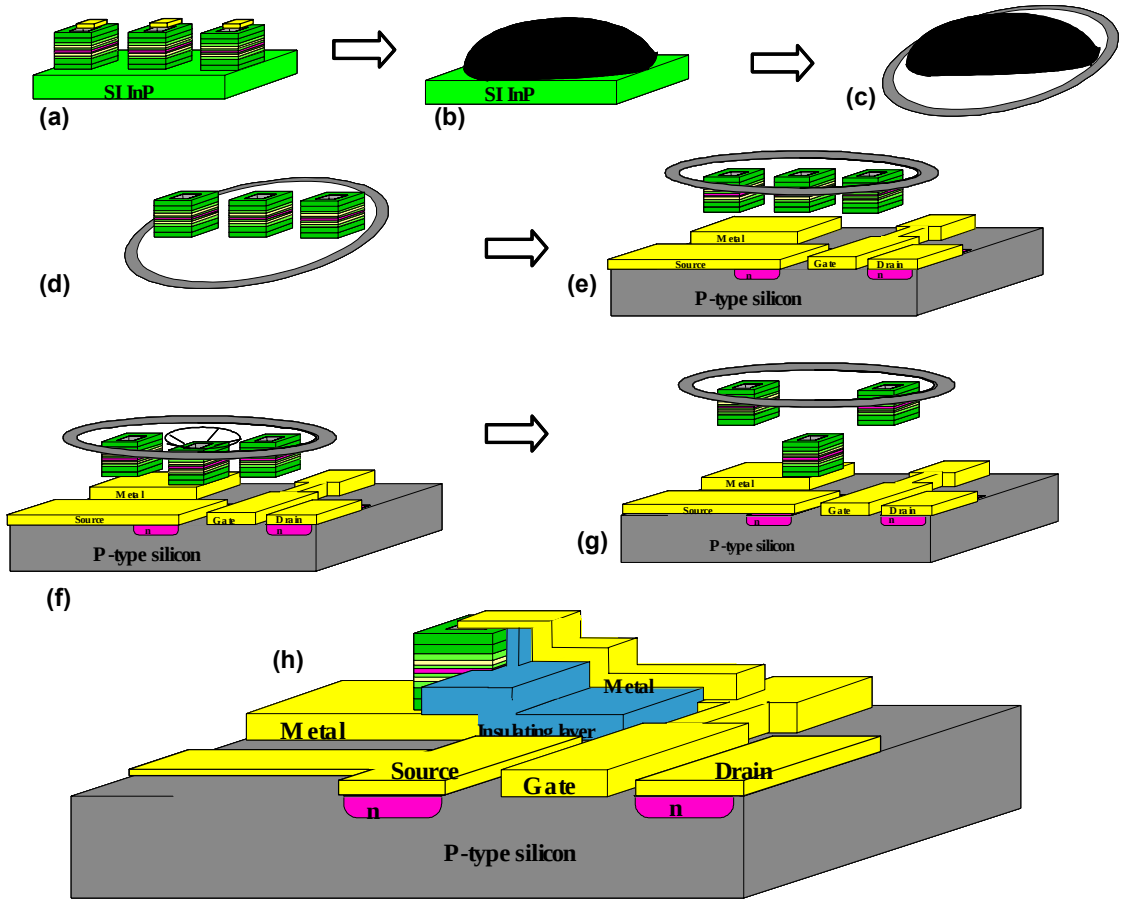


Figure 3.7 Outline of the thin-film integration for InP-based devices onto CMOS chips.

3.2.1. Planarization of the InP-based RTDs

In the alignable thin-film transfer process illustrated in Figure 3.7, the RTD is flipped before transfer. To insure good contact to the metal pad on the host substrate, the top surface of the thin-film structure to be transferred should be planar. This need for planarity was not a concern in prior work in which planar devices such as PIN diode or MSM photodetectors were integrated, but it poses a problem for a small mesa device like the RTD. Therefore, process development effort to planarize the InP-based RTDs before substrate removal was required.

The prefabricated RTDs were processed by the Applied Research Labs of Texas Instruments, Inc. (later Raytheon TI Systems) in their III-V clean room facilities. Contacts were patterned with contact photolithography in sizes ranging from $2 \times 2\ \mu m^2$ to $24 \times 24\ \mu m^2$. Ti/Pt/Au contacts were formed by e-beam evaporation and lifted off in acetone. A self-aligned timed mesa etch followed using H_2SO_4: H_2O_2: H_2O (1: 8: 160). A thin 500 Å layer of PECVD Si_3N_4 was deposited for passivation. The thickness was held to 500 Å due to initial concerns about stress in the nitride film straining the thin-film structure when the substrate was removed. Via holes were then pattered, followed by a via etch to the top of the RTD using a CF_4/O_2 plasma etch. Finally, interconnects with $100 \times 100\ \mu m$ Ti/Au contact pads were patterned, evaporated, and lifted off in order to allow for on-wafer testing of the individual devices. It should be noted $2 \times 2\ \mu m^2$ RTDs did not yield, and as a result the smallest RTD available were $4 \times 4\ \mu m^2$ RTDs. The minimum geometry RTDs did not yield because the 1 μm via hole through the Si_3N_4 to RTD top contact did not open on account of insufficient resolution of the contact aligner

photolithography. A photomicrograph of the initial on-wafer RTDs is shown in Figure 3.8 with a profile of the as-delivered RTD.

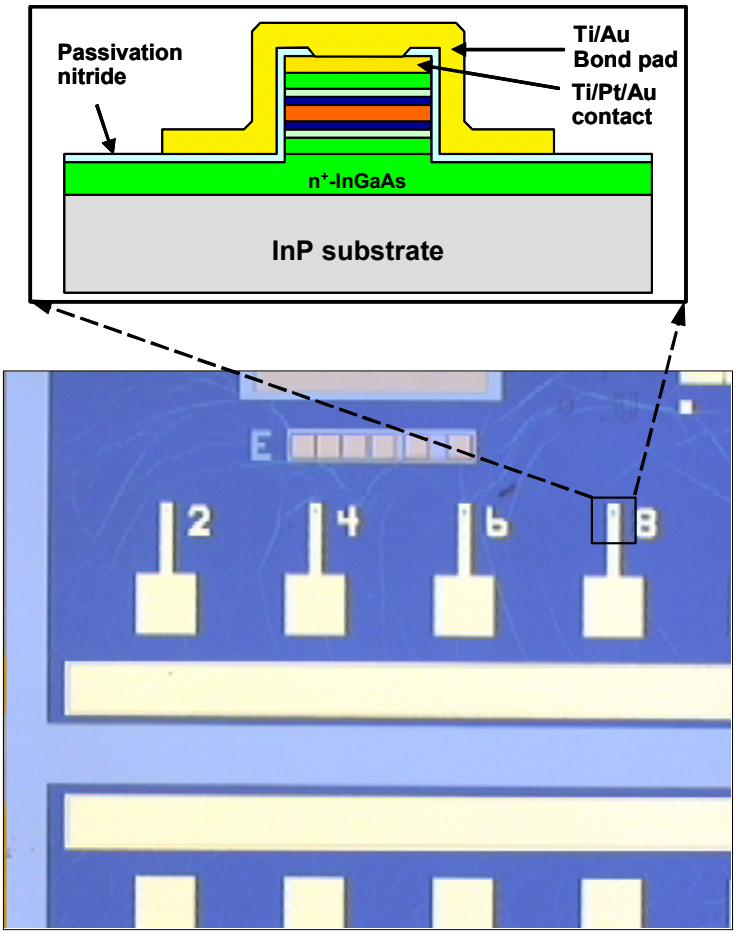


Figure 3.8 Photomicrograph of the as-delivered InAs/$In_{0.53}Ga_{0.47}As$/AlAs/$In_{0.52}Al_{0.48}As$ RTDs on InP with representative cross-section (inset).

The first step in the planarization of the RTDs is the removal of the large Ti/Au bonding pad with wet chemical etching (Figure 3.9(b)). The approximately 3000 Å of gold was etched using the iodine gold etchant (40g KI: 10g I_2: 40 mL H_2O), followed by a quick etch in dilute HF (10% by volume in H_2O) to strip the titanium. A 3 μm planarizing layer of polyimide was spin coated and cured in a nitrogen-purged furnace for 1 hour at 350 °C. In addition to planarizing the top surface of the thin-film device for good bonding, the polyimide layer partially reduces the parasitic capacitance between the top contact and the back n-InGaAs contact layer. The 3μm polyimide also greatly improves the mechanical integrity of the thin-film structure, preventing the structure from bowing as was observed in early experiments without the polyimide process. A via mask was patterned surrounding the RTD mesa by contact lithography, and the via pattern was wet etched in an aluminum etch mask. The via hole was patterned in the polyimide with an oxygen plasma etch at 300 mTorr pressure with an RF power of 300 Watts (Figure 3.9(c)). A Ti/Au layer was sputtered and the bond pads of 95 × 95 μm were patterned and wet etched (Figure 3.9(d)). Next, the field polyimide and Si_3N_4 were plasma etched in oxygen and SF_6/O_2 plasmas, respectively. Finally, the bottom n-$In_{0.53}Ga_{0.47}As$ was wet etched down to the InP substrate layer to isolate each RTD thin-film structure. The final on-wafer structure is shown in Figure 3.9(e, f), with the individual RTD structures linked only by the InP substrate, which is to be removed.

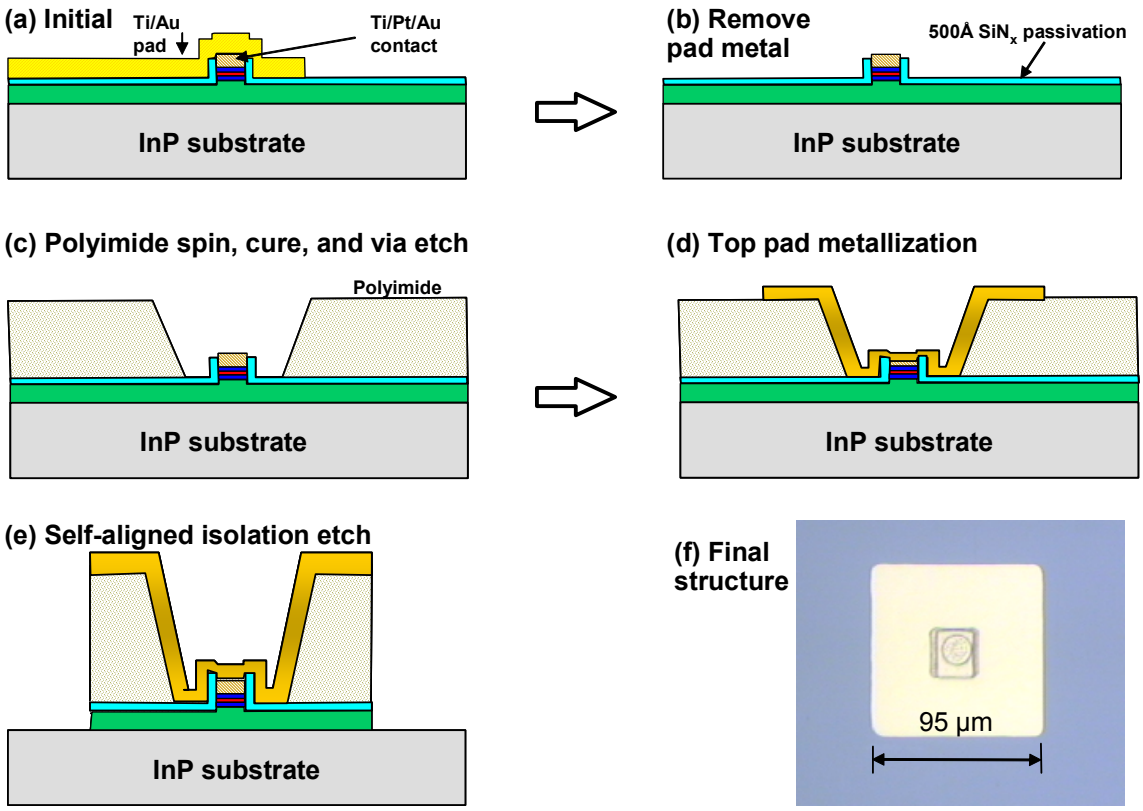


Figure 3.9 Summary of the InP-based RTD planarization process.

3.2.2. Substrate removal and transfer

Once the InP-based RTDs have been planarized and isolated, the transfer and integration process is equivalent to those outlined in. [30]-[32]. The overall scheme in the context of RTD-CMOS thin-film integration is summarized in Figure 3.10. A 100×100 µm integration bond pad and interconnect was patterned on the foundry CMOS chip prior to transfer of the thin-film RTD, followed by evaporation and lift off of Ti/Pt/Au. The CMOS chip prior to RTD transfer is shown in Figure 3.11(a). It should be noted that in the planarized RTD transfer process, the sizes of the transferred thin-film RTD die and the integration bond pad were scaled down substantially from the first experimental runs, going from 200×300 µm die and pad sizes to the 100×100 µm

dimensions shown here. This was an important development because pads of the latter size have interconnect-substrate parasitic capacitance on the order of 10 fF which would be impossible with the larger pads and die. Figure 3.11(b) shows a photomicrograph the same chip immediately following the thin-film RTD transfer and bonding.

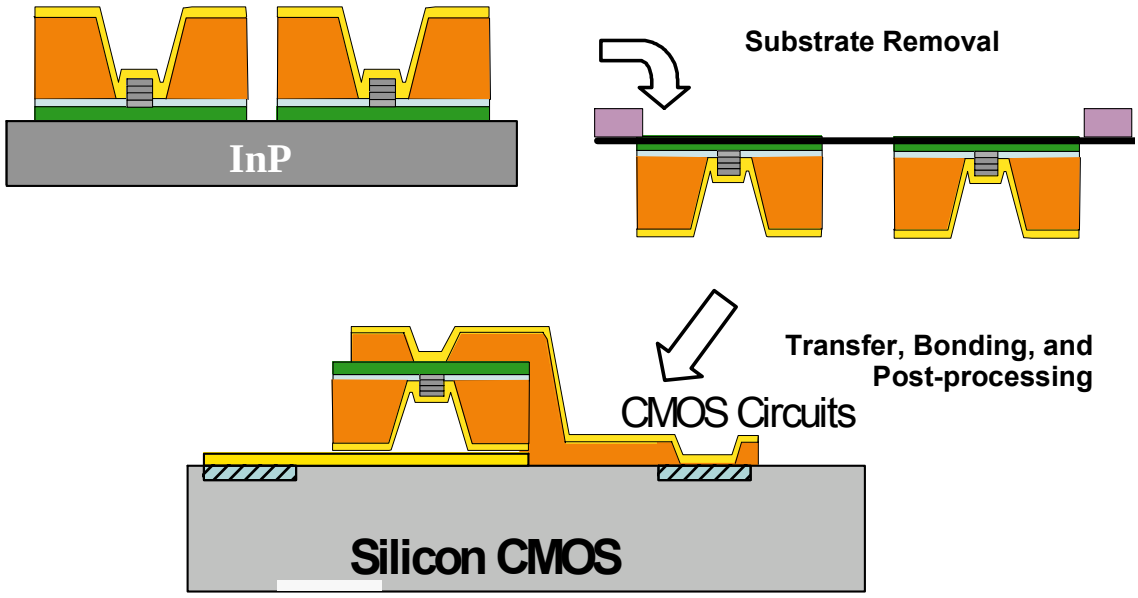


Figure 3.10 An overview of the transfer and integration of the thin-film RTD to CMOS circuits.

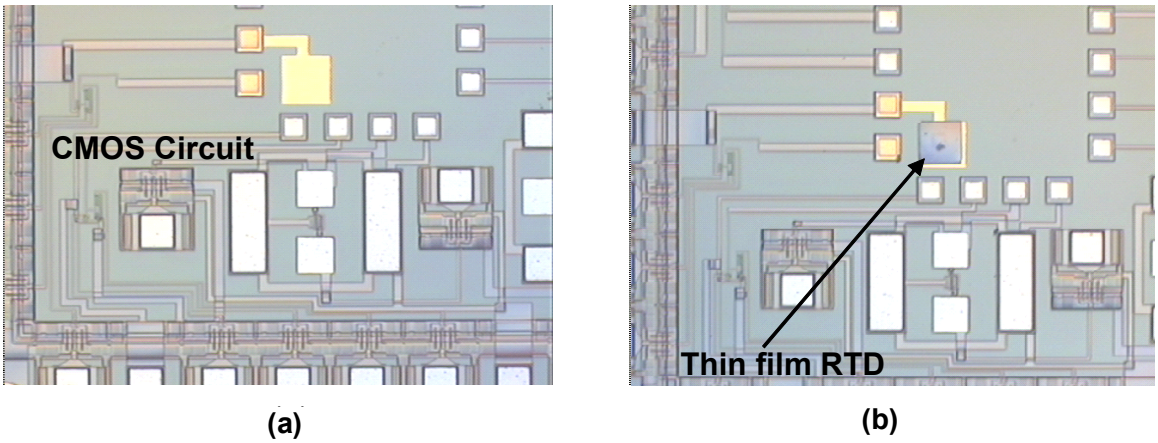


Figure 3.11 (a) Photomicrograph of a CMOS chip with Ti/Pt/Au interconnect and bond pad. (b) The same chip after transfer and bonding of the thin-film RTD.

3.2.3. Post-transfer processing of the RTD-CMOS chip

After the thin-film RTD was transferred and bonded, a polyimide layer of approximately 3µm thickness was spun and cured at 350 °C in a nitrogen-purged furnace for one hour. This polyimide layer serves as an interlayer dielectric (ILD) for the second contact between the RTD and the CMOS circuit. An aluminum mask layer was deposited, and vias over the device and the second CMOS pad were patterned in the mask layer by contact photolithography. The vias were etched using the same oxygen plasma etch as used to etch the vias in the planarization polyimide for the thin-film RTD described in Section 3.2.1. The interconnect that connects the second terminal of the RTD to the CMOS circuit pad was patterned and metallized in Ti/Au. Finally, the field polyimide was etched in oxygen plasma as described above, with the Ti/Au interconnect masking the ILD polyimide underneath it, as illustrated in Figure 3.10. A photomicrograph showing the final integrated RTD-CMOS chip is shown in Figure 3.12. The current-voltage characteristic of a 4 × 4 µm RTD tested before the start of processing

and after the full integration process is shown in Figure 3.13, along with the epitaxial layer structure of the particular RTD wafer used for RTD-CMOS integration. The thin-film integrated RTD's DC characteristic shows a slight increase in series resistance but the RTD is not otherwise degraded.

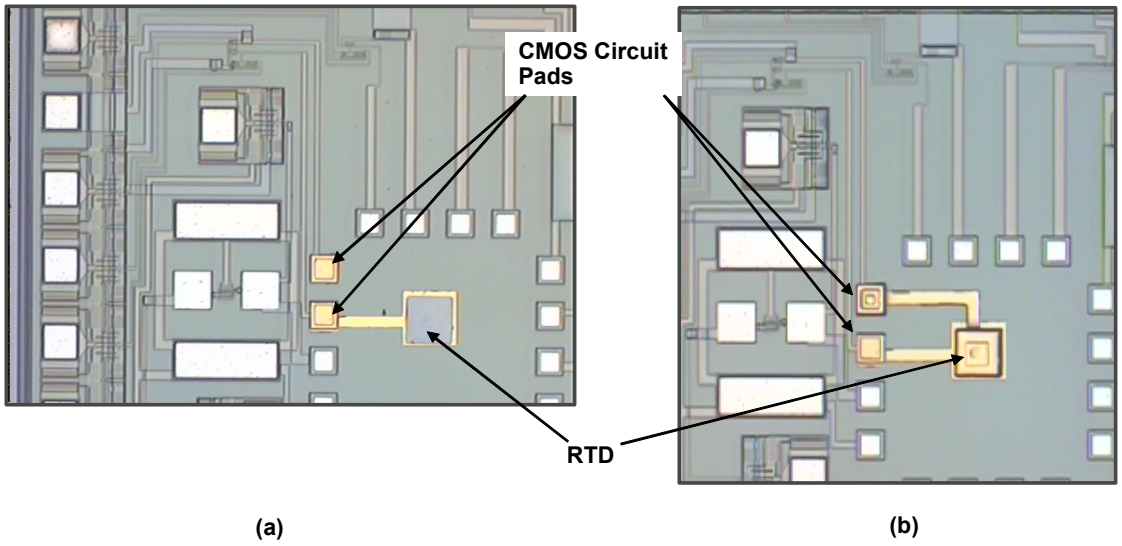
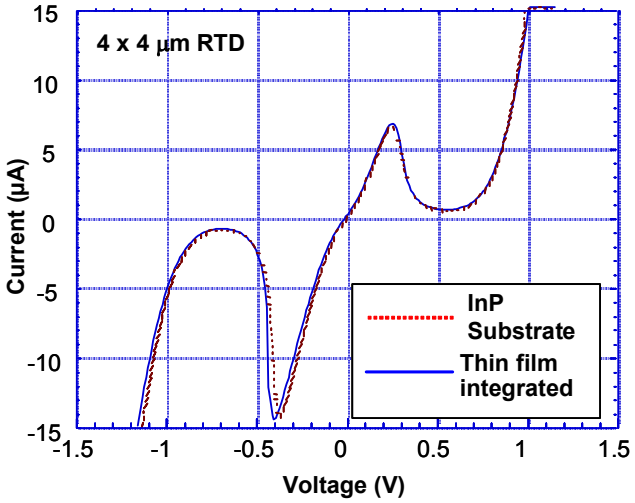


Figure 3.12 (a) RTD-CMOS chip immediately after transfer of the thin-film RTD. (b) The final integrated RTD-CMOS chip.

	Composition	Thickness (Å)	Doping (cm^{-3})
13	$In_{0.53}Ga_{0.47}As$	1000	5E18
12	$In_{0.53}Ga_{0.47}As$	1000	1E18
11	$In_{0.53}Ga_{0.47}As$	40	
10	$In_{0.52}Al_{0.48}As$	25	
9	AlAs	25	
8	$In_{0.53}Ga_{0.47}As$	15	
7	InAs	25	
6	$In_{0.53}Ga_{0.47}As$	15	
5	AlAs	25	
4	$In_{0.52}Al_{0.48}As$	25	
3	$In_{0.53}Ga_{0.47}As$	40	
2	$In_{0.53}Ga_{0.47}As$	1000	1E18
1	$In_{0.53}Ga_{0.47}As$	5000	5E18
0	InP substrate		

(a)



(b)

Figure 3.13 (a) Epitaxial layer structure of the RTDs used in RTD-CMOS integration. (b) A representative RTD's I-V curves shown before processing and after the full integration to a CMOS chip.

3.3. RTD-CMOS Demonstrations

3.3.1. RTD-nMOS building blocks

The drain-loaded RTD-nMOSFET and the gate-loaded RTD-nMOSFET were alluded to in Chapter 2 as essential components of RTD-CMOS digital and mixed-signal circuits. Both structures were demonstrated using the thin-film integration method detailed in Section 3.2.

In the case of the drain-loaded RTD-nMOSFET, which functions as a static RTD-CMOS Schmitt-inverter, the margin is determined by the PVCR of the RTD, and the relative match between the RTD current and the current drive capability of the nMOSFET. The integrated RTD I-V characteristic of the device in the RTD-nMOSFET Schmitt-trigger is shown in Figure 3.14(a), with the measured inverter transfer curve shown in Figure 3.14(b).

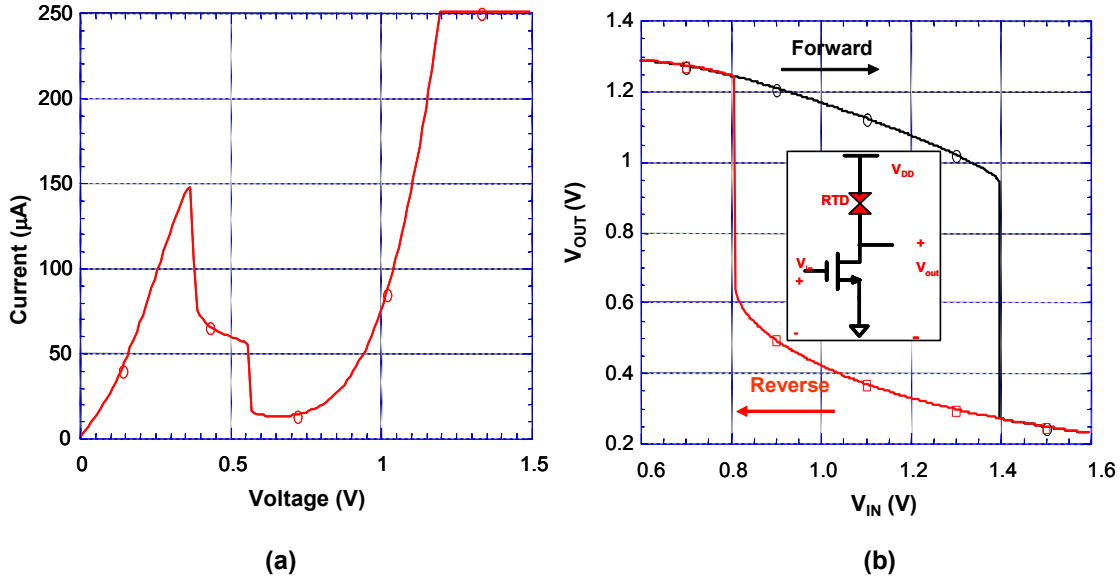


Figure 3.14 (a) I-V curve for the RTD integrated to the static RTD-nMOSFET inverter. (b) Transfer curve of the RTD-nMOSFET Schmitt-triggered inverter.

The gate-loaded RTD-nMOSFET current amplifier shown in Figure 5.1(b), when the injected current into the RTD exceeds its peak current threshold, the RTD switches to its high voltage state. Since this is above the nMOSFET's threshold voltage of approximately 0.7 volts, the nMOSFET is switched from off to on. The measured transfer curve is shown in Figure 3.15(a), using an external current source as the load (with voltage compliance set at 3 volts) and compares well with the simulated curve shown in Figure 3.15 (b).

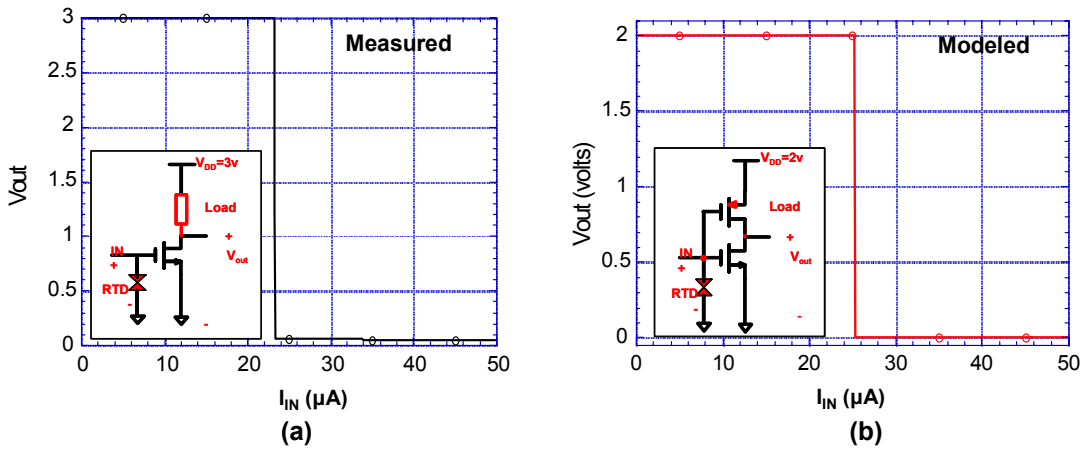


Figure 3.15 (a) The measured transfer curve of the RTD-nMOS current amplifier. (b) Simulated curve transfer curve of the RTD-nMOS current amplifier.

3.3.2. RTD-CMOS comparator

Using the hybrid thin-film integration process described in Section 3.2, the world's first resonant tunneling CMOS integrated circuit was demonstrated [49]. The RTD-CMOS comparator schematic is shown in Figure 3.16(a), with the sinusoidal input voltage provided by an arbitrary waveform generator. The voltage source is translated into a near sinusoidal current by the current mirror, which provides a resistive load to the waveform generator. In this circuit, the nMOSFET is clocked to externally reset the RTD. The circuit is externally biased with a source measurement unit to a power supply voltage of 5 volts.

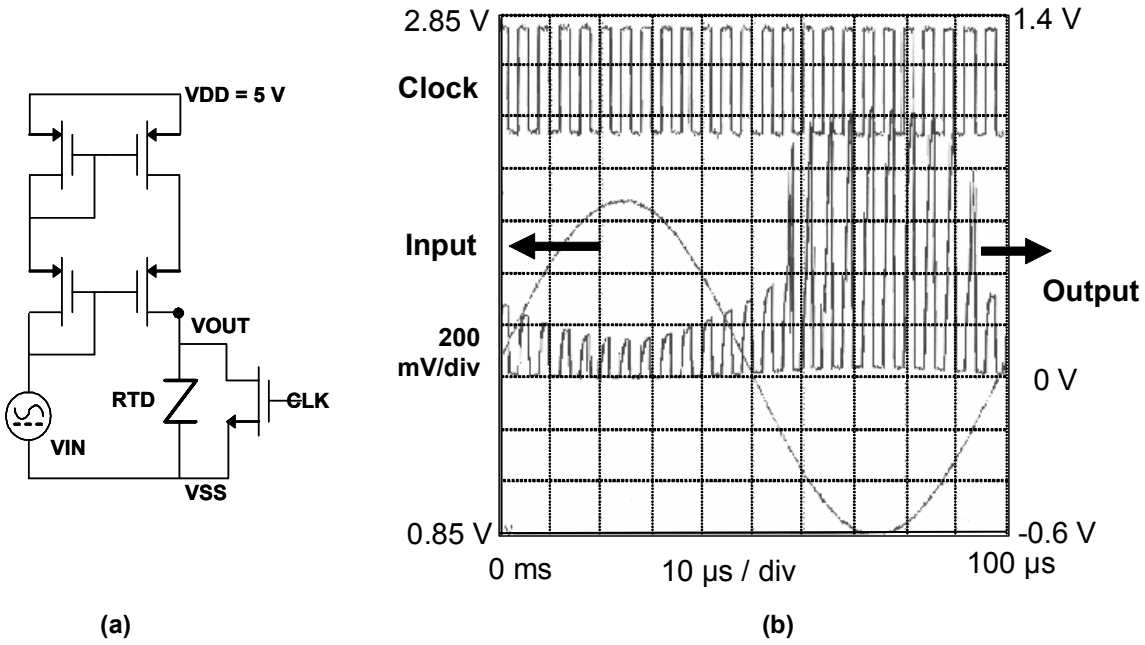


Figure 3.16 (a) Circuit schematic of the RTD-CMOS comparator as tested. (b) Output waveform generated by the RTD-CMOS comparator.

When the injected current from the input causes the total RTD current to exceed its peak current, the circuit switches to the high voltage state and latches. The RTD I-V peak current for this circuit is 98 µA. The external clock resets the comparator to the low voltage state. The response of the circuit with a sinusoidal input is shown in Figure 3.16(b). The response agrees well with simulation. The sinusoid superimposed on the output is present because no buffering output stage, such as a CMOS inverter, is used as was the case in the simulation in Chapter 2. The abrupt transition of the output is clearly shown at the threshold voltage of 1.1 volts, demonstrating the comparator's potential for application in high sensitivity receivers.

CHAPTER 4

OPTIMIZING THE RTD FOR THIN-FILM INTEGRATION

4.1. Proposed Modifications for Thin-Film RTD Structures

To truly benchmark RTD/CMOS technology relative to all-CMOS technology, the parasitic capacitance associated with the integration of RTDs to CMOS must be improved. There is a large parasitic capacitance associated with the thin-film RTD structure shown in Figure 3.9(e) due to the need for the via through the polyimide to overlap the RTD mesa. This results in a very large parallel plate capacitance through the 500 Å SiN_x layer to the n-$In_{0.53}Ga_{0.47}As$ RTD contact layer. While the bottom integration pad and interconnect have a large parasitic capacitance, it is typically connected to a power line or the circuit ground in most circuit designs, where the extra capacitance is not an problem because the voltage is not being switched. The capacitance associated with the top interconnect is important since the voltage at this node needs to be switched, and switching time scales with the total node capacitance. This capacitance is at least an order of magnitude below that of the bottom integration pad and interconnect because it is smaller in area and has an additional layer of 3-5 μm polyimide insulating layer over the overglass that separates the interconnect from the conductive silicon substrate. Some circuit designs, however, require low capacitance at both terminals of the RTD, which requires an improved process. Another drawback of the current process is the need for substantial post-processing after bonding of the thin-film RTD die, which becomes a challenge if multiple RTDs are to be integrated. To address these issues, two modified

thin-film integration schemes are proposed: the back-contacted RTD with etch stop and the front-only contacted RTD.

The concept of back-contacted thin-film RTD is illustrated in the simplified process flow diagram of Figure 4.1. In general, the process is identical to that described in Chapter 3, but it differs in two essential details. A thin 30 Å n^+-doped InP etch stop layer is inserted into the RTD epitaxial layer stack beneath the n-$In_{0.53}Ga_{0.47}As$ lower RTD terminal (Figure 4.1(a)). Since the barrier height between $In_{0.53}Ga_{0.47}As$ and InP is only 0.2 eV, the insertion of the thin etch stop layer does not adversely affect the electron transport. The planarized RTDs can then be fabricated without process modifications (Figure 4.1(b)). The substrate can be removed conventionally with HCl: H_3PO_4 selectively etching the InP substrate but stopping on the lowest n-$In_{0.53}Ga_{0.47}As$ epitaxial layer (Figure 4.1(c)). Before bonding the thin-film to the transfer diaphragm, the thin-film is transferred to another selective etch to remove the n-$In_{0.53}Ga_{0.47}As$. Both the H_2SO_4: H_2O_2: H_2O (1: 8: 160) and citric acid: H_2O_2 etchants etch $In_{0.53}Ga_{0.47}As$ with very high selectivity to InP so that a 30 Å InP layer would be sufficient to serve as a reliable etch stop when removing the n-$In_{0.53}Ga_{0.47}As$. The removal of this parasitic capacitance eliminates the large parallel plate capacitance between the SiN_x and the n^+-$In_{0.53}Ga_{0.47}As$ contact layer (Figure 4.1(d)). The remainder of the thin-film integration process proceeds without modification from the baseline process (Figure 4.1(e)).

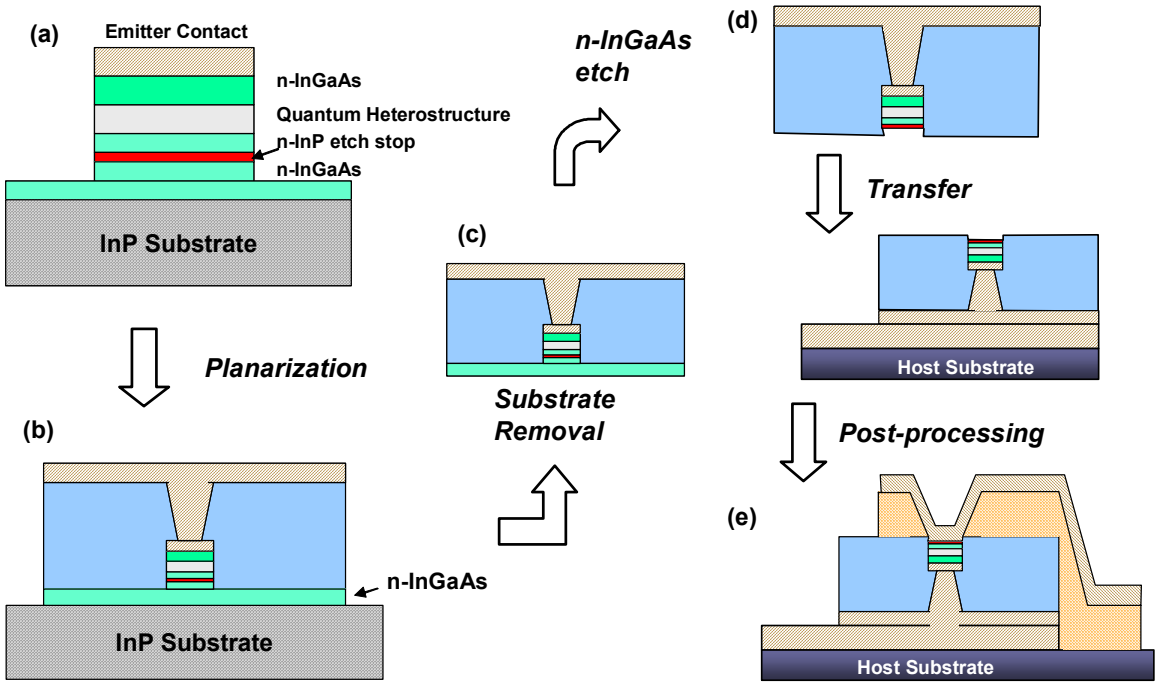


Figure 4.1 The modified back-contacted thin-film RTD integration process.

The front-side-only thin-film RTD integration scheme is pictured in Figure 4.2, and is similar to the method used for thin-film integration of inverted MSM photodetectors to receiver circuits [32], [50], [51]. In this case, a more complex fabrication process is needed to planarize the RTD structure and to form contact pads to both RTD terminals on the top surface of the planarizing dielectric. Some additional pre-transfer processing must also be carried out on the silicon host chip. Specifically, the integration bond pad on the host chip must be placed on top of an additional ILD because the parasitic capacitance between the circuit interconnect and the conductive silicon substrate could never be acceptably low if the interconnect and bond pad were placed directly on the SiO_2 overglass. This front-side-only method has the advantage, however, of eliminating the post-integration processing required to contact the back terminal of the

RTD. Finally, this process allows multi-RTD thin-film structures to be more easily integrated.

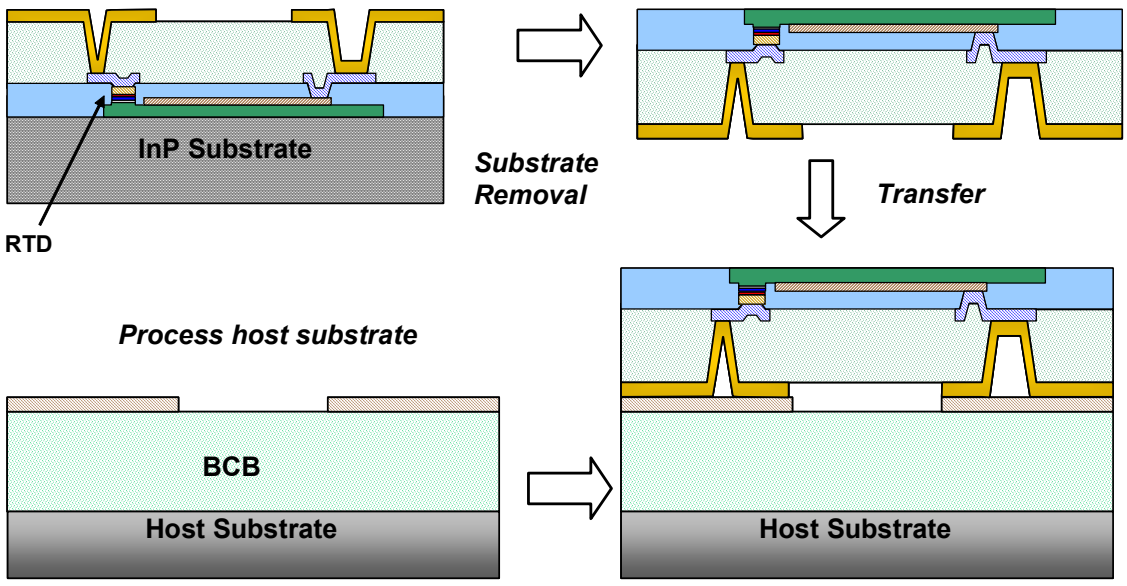


Figure 4.2 The front-side contacted RTD integration process.

The relative advantages and disadvantages of the back contacted thin-film integration with etch stop vs. the front-side-only integration are summarized in Table 4.1. An additional potential benefit of the front-side-only contact is the option of an optical input to the device such as for an optical RTD photodetector [52].

Table 4.1 Summary of the relative advantages and disadvantages of the back contact with etch stop and front-side-only contact thin-film RTD integration methods

	Back contact with etch stop	Front-side only contact
Host Substrate Processing	Minimal	Substantial
Post-processing requirements	Substantial	Minimal
Optical Input	None	back-illumination
Multiple Terminals	No	Yes

4.2. Next Generation Thin-Film RTD Process Overview and Analysis

4.2.1. Improvements in the RTD fabrication process

The layout and cross-section of a representative next generation front-side-only contacted RTD are shown in Figure 4.3. The device fabrication process was designed to implement proven IC fabrication technology based on the monolithic nanoelectronic circuits built on InP substrates [53].

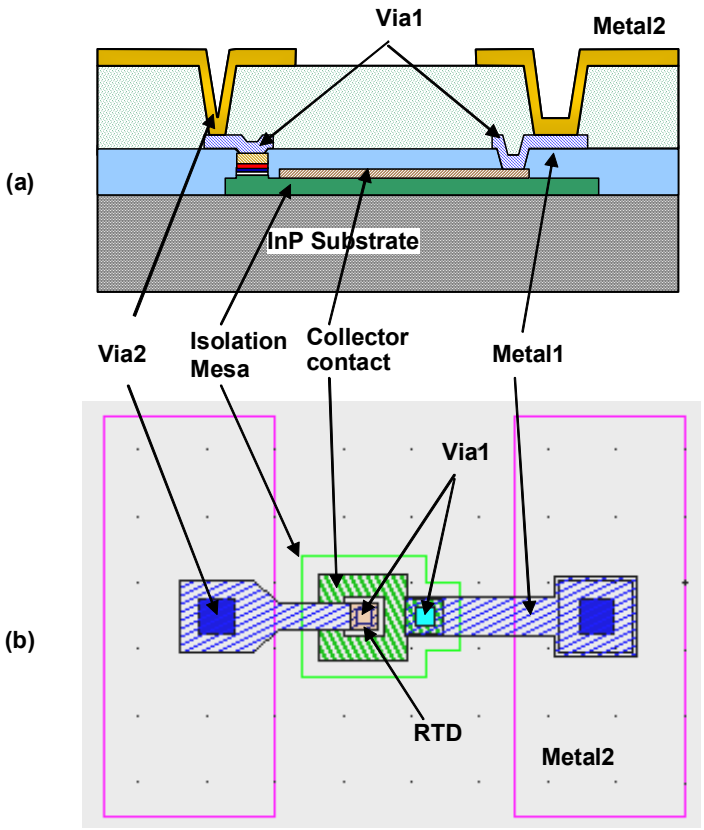


Figure 4.3 (a) Cross-sectional and (b) top view schematics of a front-side contacted next generation thin-film RTD.

There were several general process modifications incorporated into the next generation thin-film RTD fabrication. First, a 5X-reduction G-line optical stepper was used instead of a contact aligner. The stepper's alignment tolerance was 0.1 µm compared with about 1 µm for the contact aligner, allowing for a reduction in the RTD minimum dimension from 4 µm to 1.4 µm, which represents an 8× reduction in diode area. This reduction in area would in turn allow for the use of RTDs with higher peak current densities, and therefore higher speed index. Second, an n-$In_{0.53}Ga_{0.47}As$ mesa etch to the InP substrate served to reduce overlap between the overlying metal interconnects and the back n-contact region. The use of a 1.0 µms spin-on glass (SOG)

as the first level dielectric instead of only a thin (< 1000 Å) SiN_x passivation layer improves the degree of top surface planarization as well as lowers the dielectric capacitance associated with this layer. Finally the second level benzocyclobutene polymer (BCB) dielectric film planarizes the top surface, improves mechanical stability of the thin-film structure, and further lowers the structure's capacitance. The benefits of these process modifications are summarized in Table 4.2.

Table 4.2 Next-generation thin-film RTD process improvements

Process Improvement	Benefit
5X optical stepper's improved alignment tolerance	Allows minimum geometry RTDs to be fabricated (1.4 × 1.4 μm)
n-InGaAs mesa etch	Reduces overlap of top overlying metal and n-InGaAs layer
SOG Passivation/Level 1 dielectric	1.0 μm thick layer lowers dielectric capacitance, with improved degree of planarization over SiN_x
BCB Level 2 Dielectric	Planar top surface and mechanical stability

Included in the mask set for the next generation RTD production were front-contact-only structures for multiple RTDs that are commonly used in RTD-CMOS designs, as listed below in Table 4.3. Each of the structures listed below is available in four different RTD device areas: $1.4 \times 1.4\ \mu m^2$, $2 \times 2\ \mu m^2$, $4 \times 4\ \mu m^2$, and $6 \times 6\ \mu m^2$.

Table 4.3. RTD structures included on the next-generation RTD mask

Structure	Number of RTDs	Number of Terminals	Type of Contact (Back or Front-only)
Single RTD	1	2	Back
Single RTD	1	2	Front-only
Asymmetric RTD Pair	2	3	Front-only
Symmetric RTD Pair	2	3	Front-only
Independent RTD Pair	2	4	Front-only
RTD Bridge	4	4	Front-only

4.2.2. Layout design rules

The development of new layout design rules is key to the development of the new RTDs. Some of these design rules are simply limited by process limitations of the semiconductor fabrication equipment being used, such as minimum RTD device area, while others are mandated by the requirements of thin-film integration. To assess the requirements of thin-film integration on the RTD structure layout, a thorough analysis of the parasitic capacitance associated with the thin-film transfer and bonding procedure was needed. First, the critical technology design rules are summarized in Table 4.3.

Table 4.4. Critical design rules for the next-generation thin-film RTD

Feature	Constrained by	Rule
RTD Size	Photolithography	= 1.4 μm
OHMIC to RTD Spacing	Photolithography alignment tolerance	=1.0 μm
VIA1 Size	Photolithography	=1.0 μm
METAL1 Thickness	Need for planarity	= 6000 Å
FOX Level 1 Dielectric Thickness	Stress; spin-on glass will crack at thickness greater than 6000 Å	= 6000 Å
BCB Level 2 Dielectric Thickness	Tradeoff between parasitic capacitance and process yield	< 3 μm
VIA2 Width	BCB thickness and via plasma etching	= 2× BCB thickness
METAL2 Width	Alignment tolerance of thin-film transfer process	= 30 μm
METAL2 Thickness	Stress	< 7000 Å

The minimum RTD size and spacing between the RTD and the ohmic contact are simply determined by the limits of the optical lithography system available. The METAL1 thickness was set to be less than 6000 Å because the hillock that it creates in the overlying BCB surface is proportional to the metal thickness. Making the METAL1 too thin, however, increases parasitic resistance and makes the METAL1 alignment marks too faint to be seen clearly when covered in BCB and masked with metal. The thickness of the spin-on glass component of the level 1 dielectric is constrained by stress because the spin-on glass is prone to crack at thickness greater than 6000 Å. Otherwise, the SOG should be as thick as possible to lower parasitic capacitance.

The thickness of the BCB was set after some careful analysis of the contribution of the integration interconnect to the overall circuit parasitic capacitance. It was found that increasing the total thickness above about 2 μm did not significantly lower the total

capacitance enough to justify the increased processing difficulty. VIA2 width was set to be proportional to the BCB thickness; a 1:2 aspect ratio is reliably achievable with the available plasma etching techniques. Finally, the METAL2 width was set to be at least 30 µm due to the alignment tolerances of the thin-film transfer to bond pads. The smaller the bond pads, the lower their parasitic capacitance. METAL2 thickness was limited to 7000 Å in order to assure that stress on the underlying BCB would not be a problem.

4.2.3. Characterizing the parasitics

As mentioned previously, to achieve high performance in RTD/CMOS circuits using thin-film integration, the parasitic capacitance associated with the integration process must be minimized. Overall parasitic capacitance due to presence of the thin-film RTD can be broken down into four fundamental contributions, irrespective of the type of integration process used (front-only or back contacted): (1) device, (2) thin-film structure, (3) integration interconnect, and (4) CMOS pad capacitances. Figure 4.4 illustrates the components of the overall capacitance in a RTD structure integrated to a silicon chip.

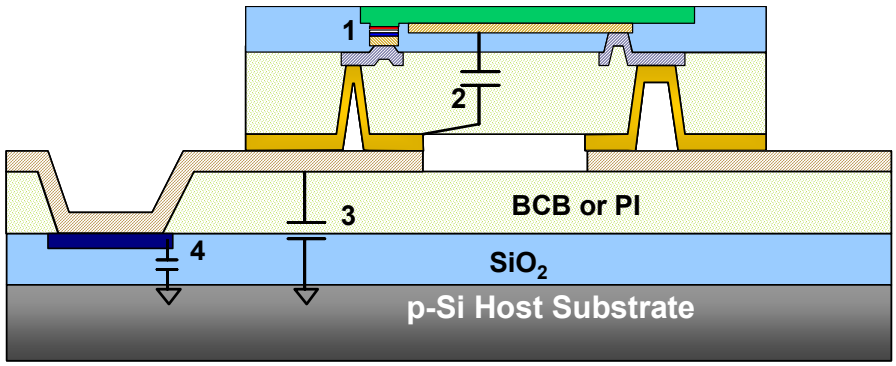


Figure 4.4 The components of the overall parasitic capacitance.

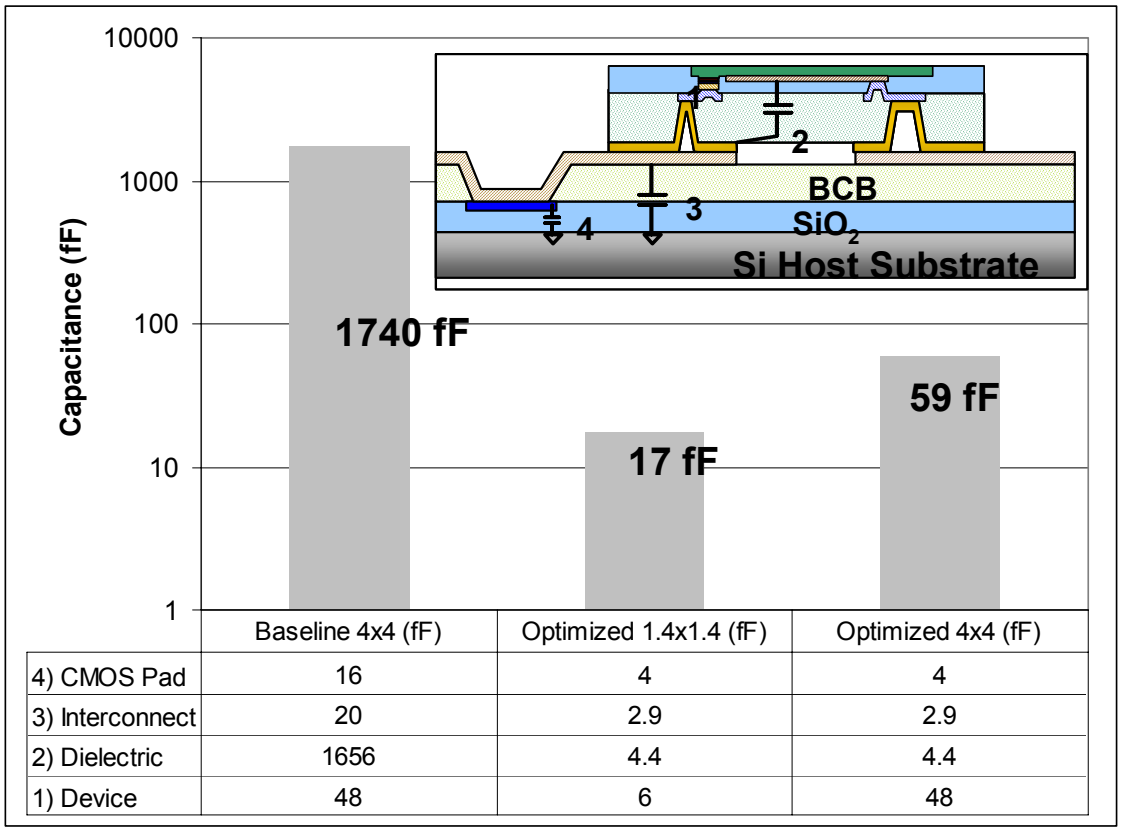
The device capacitance ranges from 2-8 fF/μm^2, depending on the specific quantum heterostructure. An improvement in device capacitance can be achieved only by scaling the RTD area from a minimum of 16 μm^2 in the original RTD wafers to a minimum of 2 μm^2 in the next generation technology. This improvement was made possible by the transition from contact print lithography to optical stepper lithography, with the latter's improved alignment tolerance.

The capacitance associated with the thin-film RTD structure in the original planarized RTD process was very high due the thin 500 Å SiN_x between the metal top pad and the n-$In_{0.53}Ga_{0.47}As$ bottom ohmic layer. This contribution to the capacitance can be reduced to negligible levels by using the SOG passivation process, by which a planarizing 1 μm oxide layer is deposited over the device. Vias as small as 1.0 microns can be etched in the oxide, allowing a via directly to the top of the RTD, resulting in very low dielectric capacitance from Metal1 to the back n-InGaAs layer. Also, the n-$In_{0.53}Ga_{0.47}As$ bottom ohmic layer is etched to form a mesa that has minimal overlap with the overlying metal layers, further reducing the capacitance associated with the thin-film structure.

The interconnect and CMOS pad capacitances are dependent on the method of integration of the RTD to the CMOS chip. In the back-contacted process of Figure 4.1, the top interconnect is insulated from the conductive silicon substrate (typically 1 – 100 Ω-cm) by both the overglass and the polyimide interlayer dielectric, resulting in a low parasitic interconnect. The improvement in parasitic capacitance can only be achieved by reducing the interconnect size, resulting in interconnect capacitances of less than 5 fF. The bottom integration pad, due to the lack of the polyimide layer for insulation and the

larger size of the pad, has a parasitic capacitance on the order of 50 fF, which is too large to serve as a signal interconnect node. For this reason, the interconnects in the front contacted process of Figure 4.2 cannot be formed directly on the overglass, even though the interconnects are smaller than the large bottom integration pad in the back contacted process. Rather, an additional layer of insulation, a BCB layer 3–6 microns thick applied to the CMOS chip before transfer of the RTD die. Vias to the CMOS pads are first etched in the cured BCB layer, and the gold integration pads are patterned on top of the BCB, as can be seen in Figure 4.4. The thickness of this layer is limited by the maximum via aspect ratio that can be reliably etched in the BCB. For a given via aspect ratio, the width of the via to the CMOS pad increases in proportion to the thickness of the BCB. The capacitance of the CMOS pad is strictly a function of the pad area, and the pad area is limited by the width of the via in the BCB. This results in a tradeoff between the CMOS pad capacitance and the interconnect capacitance. For a via aspect ratio of 2:1, the minimum overall capacitance was found to coincide with a BCB thickness of about 5 μm, which results in minimum CMOS pad dimensions of 20×20 μm. A safe size of 40×40 μm was chosen in early designs, but the transition to 20×20 μm pads would reduce the pad capacitance to below 4 fF.

Figure 4.5 shows a comparison of the overall capacitance of an integrated RTD in both the original and next generation back contacted RTD process. The rather high capacitance associated with the original structure is dominated by the capacitance through the 500 Å SiN_x.



	Baseline 4x4 (fF)	Optimized 1.4x1.4 (fF)	Optimized 4x4 (fF)
4) CMOS Pad	16	4	4
3) Interconnect	20	2.9	2.9
2) Dielectric	1656	4.4	4.4
1) Device	48	6	48

Figure 4.5 The distribution of the total parasitic capacitance for the integrated RTD strucutre.

The overall estimated capacitance distribution is detailed in Figure 4.6 for the single front contacted RTD for the four different device sizes included in the next generation RTD mask set. The capacitance is dominated by the intrinsic RTD capacitance for devices sized greater than $2 \times 2\ \mu m^2$. Figure 4.7 details the overall capacitance per interconnect with minimum geometry RTDs for several different structures included in the mask set.

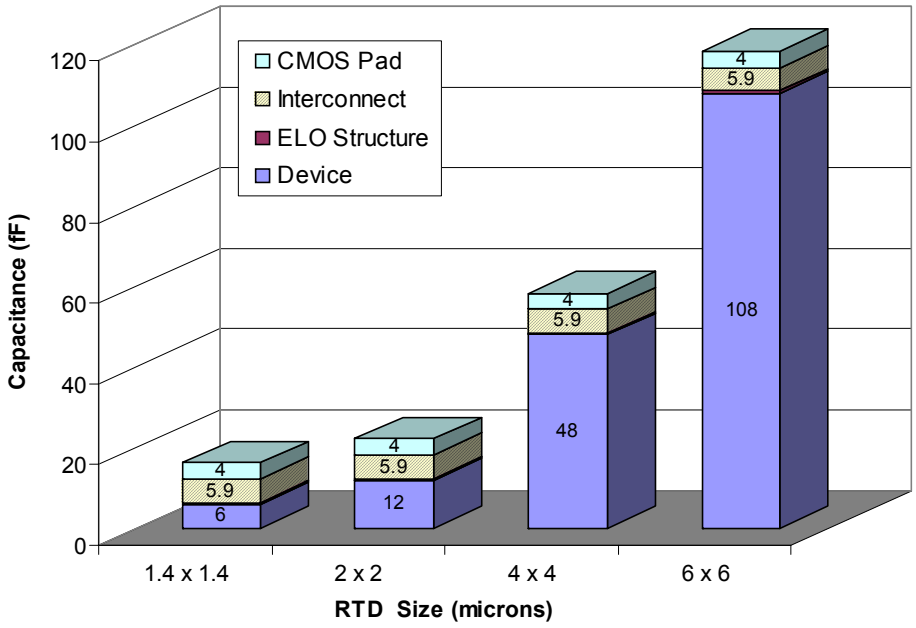


Figure 4.6 The calculated overall capacitance of the integrated front-contact RTD, with each component shown individually.

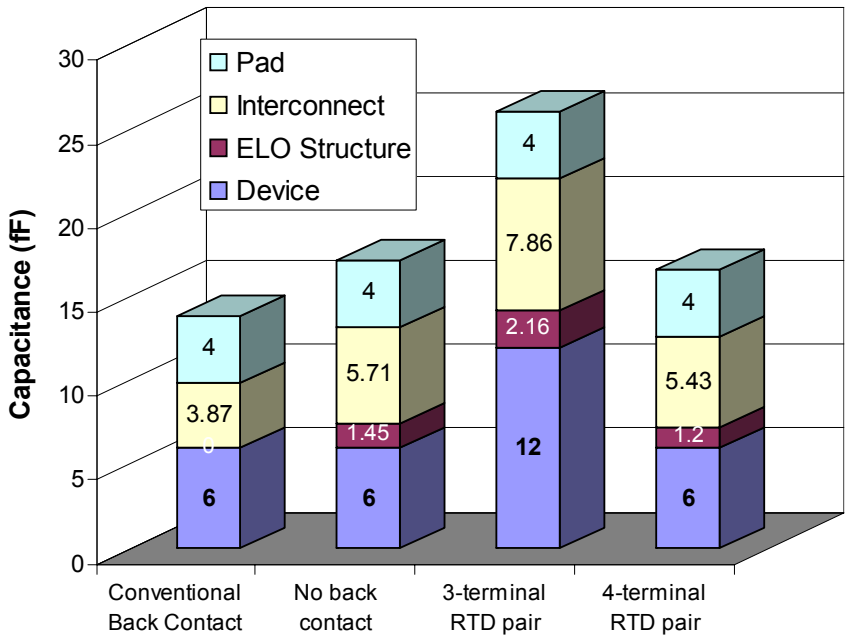


Figure 4.7 The distribution of capacitance per interconnect for different thin-film RTD structures that employ minimum geometry $1.4 \times 1.4\ \mu m^2$ RTDs.

4.3. Fabrication of Next Generation Thin-Film RTDs

The detailed process flow for the fabrication of the next generation RTDs is summarized in Figure 4.8, which is referred to in the following subsections that detail each specific step.

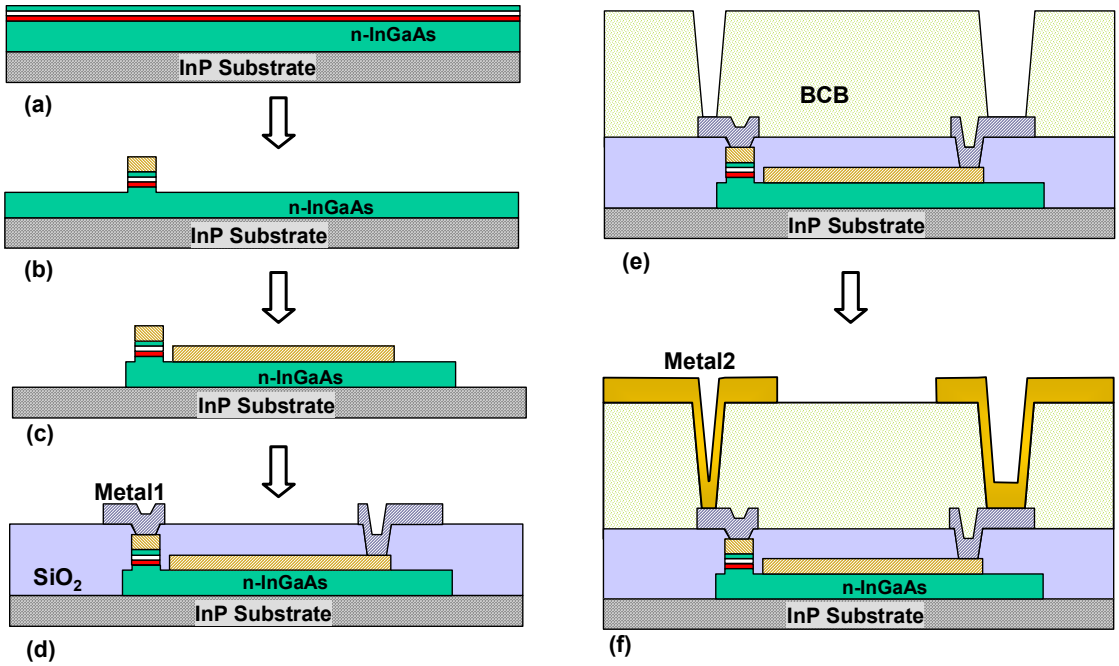


Figure 4.8 The next generation RTD fabrication process flow.

4.3.1. Epitaxial Growth (Figure 4.8(a))

Five 3-inch InP substrate epitaxial wafers were grown using solid source molecular beam epitaxy (MBE). In order to vary the RTD peak current density of each wafer, each epitaxial layer structure included a different barrier thickness. The peak current density was designed to range from 0.5 to 60 kA/cm^2. Shown in Table 4.5 is a typical RTD layer structure; the only variation between wafers was the inclusion and thickness of a lattice-matched InAlAs pre-barrier to lower the peak current density. The 100 Å n-InP layer serves as an etch stop, though it is not necessary in this process due to the isolation etch of the bottommost n-$In_{0.53}Ga_{0.47}As$ layer in step (c).

Table 4.5 A representative epitaxial layer structure of the RTDs fabricated

	Composition	Thickness (Å)	Doping (cm^{-3})
13	$In_{0.53}Ga_{0.47}As$	1000	1E19
12	$In_{0.53}Ga_{0.47}As$	200	1E18
11	$In_{0.53}Ga_{0.47}As$	25	
10	AlAs	25	
9	$In_{0.53}Ga_{0.47}As$	10	
8	InAs	20	
7	$In_{0.53}Ga_{0.47}As$	10	
6	AlAs	25	
5	$In_{0.53}Ga_{0.47}As$	25	
4	$In_{0.53}Ga_{0.47}As$	200	1E18
3	$In_{0.53}Ga_{0.47}As$	1000	1E19
2	InP	100	1E19
1	$In_{0.53}Ga_{0.47}As$	5000	1E19
0	InP substrate		

4.3.2. RTD emitter patterning (Figure 4.8(b))

The RTD device mesa itself was patterned using a self-aligned etch process, in which the RTD top contact serves as the etch mask. The contact was fabricated using a nitride-assisted liftoff technique, in which a 3000 Å SiN_x layer is deposited by PECVD before photoresist is spun and patterned. After photolithography, the nitride is etched and undercut, which assures a clean liftoff. The wafers were exposed to a 30 second argon sputter etch and then a 100 Å TiW sputter deposition, all while in a high vacuum to ensure a clean metal-semiconductor junction for a good ohmic contact. A Ti/Pt/Au/Ti layer of 400/400/2800/600 Å thickness was evaporated before the resist was lifted of in acetone. The Si_3N_4 layer is removed in buffered HF.

The dimensions of the RTDs are 1.4×1.4, 2×2, 4×4, and 6×6 μm^2. To achieve the minimum geometry scaling, anisotropic dry etching must be employed to

pattern the RTDs. Due to the difficulty of RIE etching of indium based semiconductors and the lack of availability of a suitable RIE system, ablative argon ion milling was employed to etch approximately 1800 Å through the RTD layers, using the Ti/Pt/Au/Ti contact as an etch mask. Experiments indicated that the ion milling exhibited an etch selectivity of approximately 3-4:1 between $In_{0.53}Ga_{0.47}As$ and titanium. This selectivity is sufficient to ensure that the contact is not severely eroded in the process. As can be seen in Figure 4.9, the current scaled almost perfectly with the drawn RTD emitter area, with practically no measurable undercut effects. In addition, good etch depth uniformity was achieved across the wafer. For this RTD wafer, the layer structure of which is described in Table 4.5, the peak current density was determined to be 16.7 kA/cm^2.

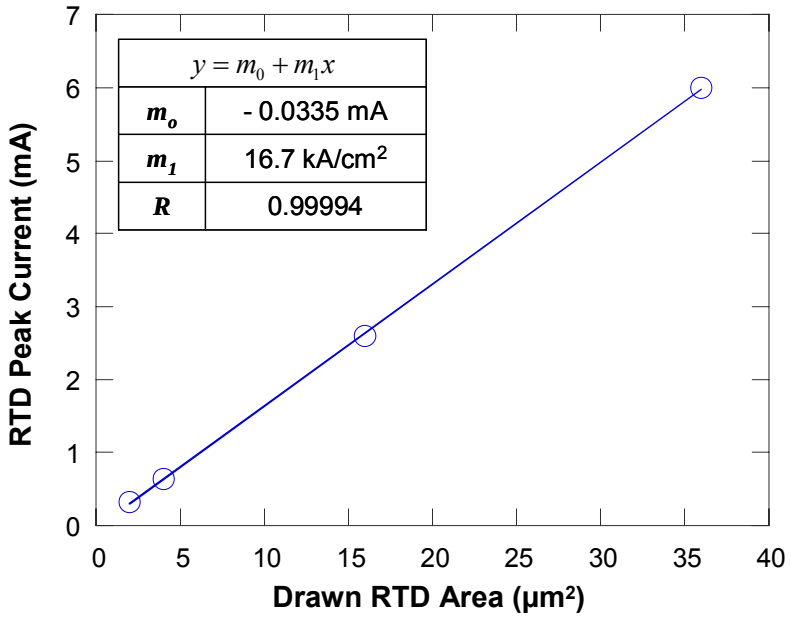


Figure 4.9 The scaling of RTD peak current with drawn area shows no effects of lateral undercut.

4.3.3. Ohmic collector contact and isolation mesa (Figure 4.8(c))

The second Ti/Pt/Au contact to the RTD was made using the same liftoff process as the emitter contact. Subsequently, an isolation mesa was patterned with conventional lithography. Because the layout design rules allowed for a large overlap of the active area, considerable undercut could be tolerated. For this reason, wet chemical etching in H_2SO_4: H_2O_2: H_2O (1:8:160) was used to etch the isolation mesa to the InP substrate.

4.3.4. SOG dielectric and first metal (Figure 4.8(d))

For passivation, a 400 Å PECVD SiN_x layer was deposited. A partially planarizing layer of SOG was spun to a thickness of 0.6 μm, followed by a deposition of 0.3 μm PECVD SiO_x. Vias to the RTD were patterned via optical stepper lithography, with a minimum dimension of 1.0 μm. The vias were etched in a CHF_3/O_2 RIE that results in a slightly sloped sidewall for good metal step coverage.

The Metal1 layer of TiW/Au/TiW was sputtered to a thickness of 1500/4000/400 Å. After patterning the Metal1 mask with photolithography, the metal layers were etched, using CF_4/O_2 RIE to etch TiW layers and argon ion milling to etch the gold.

4.3.5. BCB level 2 dielectric and via2 etch (Figure 4.8(e))

Before the BCB polymer was spun, a thin (400 Å) Si_3N_4 layer was deposited in order to improve adhesion between the BCB and the underlying TiW and SiO_x. The BCB resin was subsequently spun to 2.4 μm and cured at 250 °C for one hour. BCB was used as the level 2 dielectric because of its low parasitic properties (K = 2.7), and its excellent planarization properties (> 90% degree of planarization).

Because BCB is an organic polymer, a photoresist mask will be eroded in the BCB RIE. For this reason a 1000 Å TiW etch mask was sputtered before Via2 lithography. The pattern was etched in the TiW mask with CF_4/O_2 RIE. To etch the vias, an O_2/CF_4 plasma etch was employed with high pressure to give a sloped and undercut sidewall profile. The TiW mask was then removed with a wet chemical etch in hydrogen peroxide.

4.3.6. Second metal patterning (Figure 4.8(f))

The Metal2 layer that composes the large bond pads was composed of TiW/Au/TiW sputtered to a thickness of 1000/5000/400 Å. The reduced TiW thickness was employed to reduce the stress associated with Metal2. Metal2 was etched in the same way as Metal1.

4.3.7. Final thin-film mesa etch

The last step before substrate removal is the etching of the BCB and oxide around the RTD structure to isolate each thin-film structure so that each one can be independently transferred. In this case, a TiW mask can't be used because it will be eroded in the oxide RIE. Instead a 1000 Å layer of Al was evaporated over a 200 Å TiW barrier layer. After the mask is patterned, the BCB and oxide were etched all the way down to the InP substrate using the same etch methods used in previous steps. The Al and TiW are subsequently removed with wet chemical etching. Figure 4.10 shows a close-up image of a finished 4×4 μm RTD fabricated in this process.

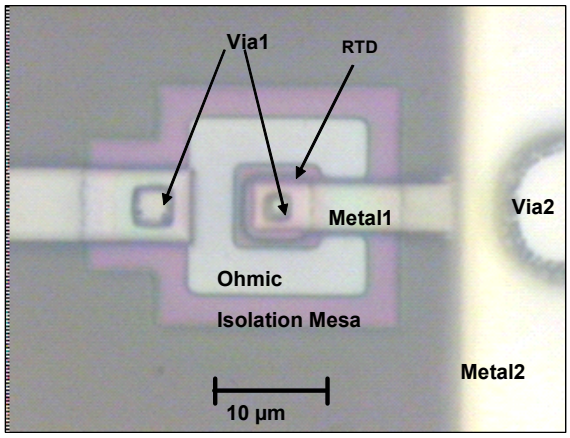


Figure 4.10. Photomicrograph of a completed 4 × 4 µm RTD.

4.3.8. Stress related problems

Subsequent to the stripping of the resist after patterning Metal2, cracks like those pictured in Figure 4.11 were observed in the BCB. Thorough experimentation showed that the crack formation occurred in the top surface of the BCB, and propagated outward from the corners of the Metal2 pattern, indicating that stress between the TiW and the BCB was the cause of the cracking. In addition, the cracks formed after exposure to the oxygen plasma used to strip the resist. To eliminate the cracking, the following process modifications were employed:

- Use only wet resist stripper after BCB is deposited, avoiding all plasma exposure.
- Use only 1000 Å TiW in the Metal2 adhesion layer to lower the associated stress.
- Add scribe lines to the Via2 pattern so that if cracks develop in isolated areas, they won't propagate beyond the subfield.
- The corners of both the Via2 and Metal2 patterns were filleted from 90° to 45° angles to reduce the stress associated with the corners of the pads.

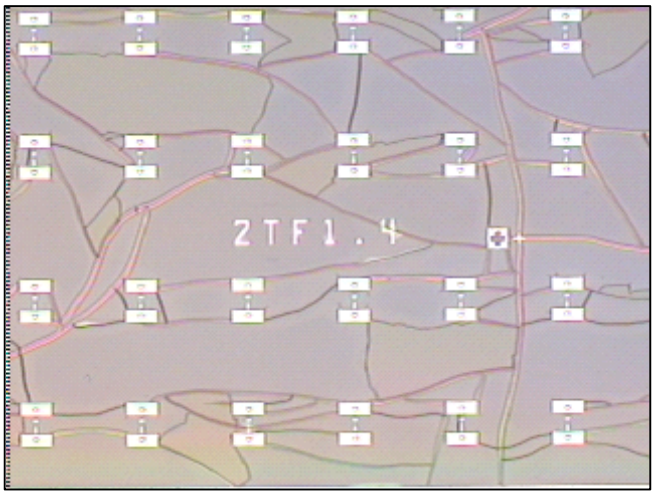


Figure 4.11 Cracks in the BCB observed on GaAs pilot wafers immediately following the patterning of the rectangular second metal bond pads

4.3.9. Uniformity and yield analysis

In order to gauge the on-wafer yield and uniformity of the next generation RTDs, the DC characteristics of one RTD of each size was tested per 10×10 mm^2 field. Three wafers from one process lot were mapped after completion of the process. In the interest of brevity, only selected results from one wafer (Wafer 4243) are included here. The interested reader can find the complete results for the wafer maps of all three wafers in Appendix B. The device level yield is 100% for all devices save the 1.4×1.4 μm^2 RTDs, as can be seen in the overlaid DC traces in Figure 4.12. The 1.4×1.4 μm^2 RTDs were expected to have the lowest yield because they require the smallest alignment and process tolerances of all the devices. Also, all of the failed 1.4×1.4 μm^2 RTDs are located in edge fields. The cause of failure for these devices is not known, but the most probable explanation is that the via overlaps the top contact of the RTD, which allows Metal1 to short the RTD.

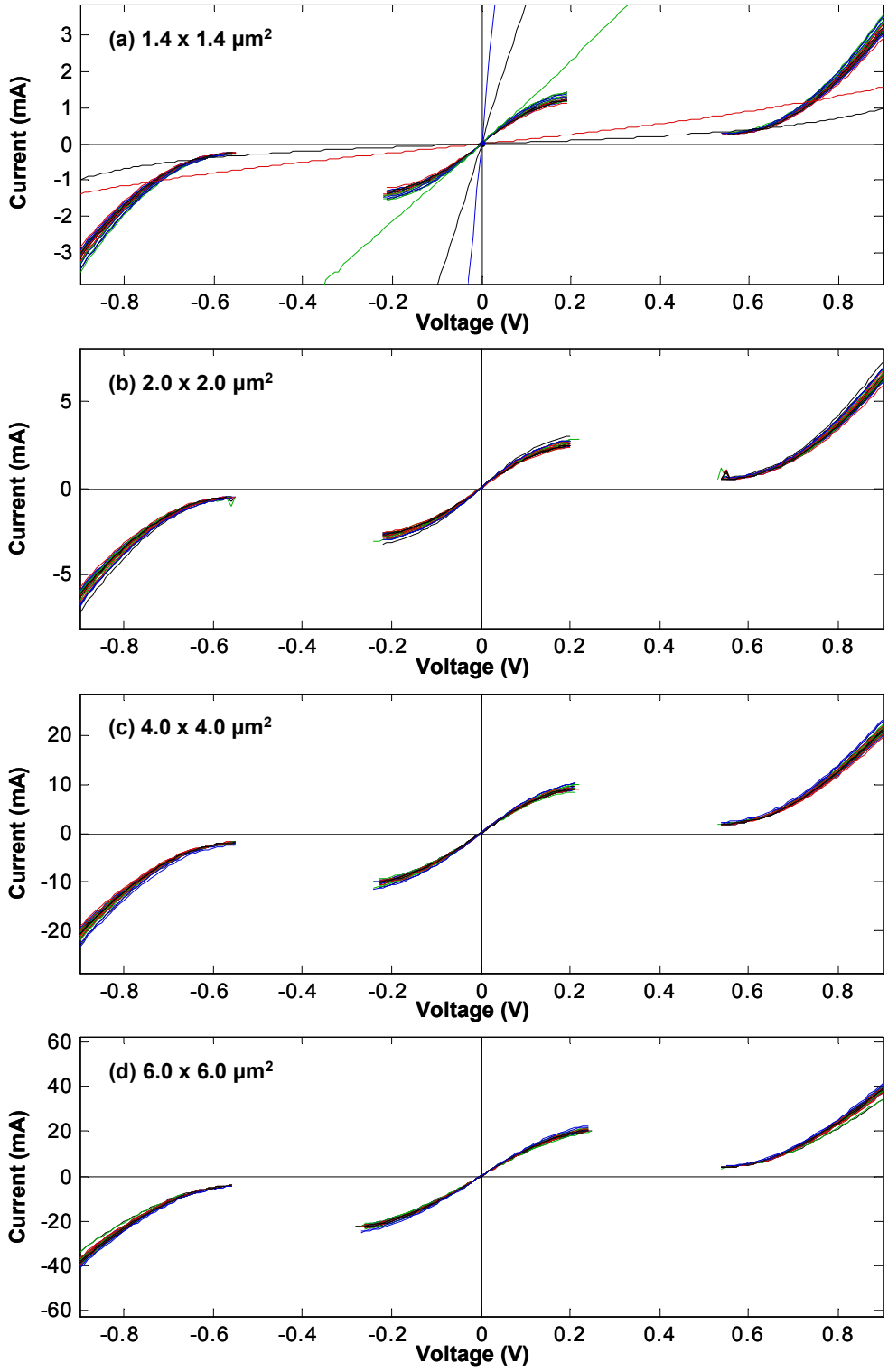


Figure 4.12. Measured I-V characteristics for next generation RTDs mapped across the three inch-wafer for devices with area (a) $1.4 \times 1.4\ \mu m^2$, (b) $2 \times 2\ \mu m^2$, (c) $4 \times 4\ \mu m^2$, and (d) $6 \times 6\ \mu m^2$.

The main variation of the RTD characteristics across the wafer is a consistent increase in the RTD peak current with respect to the wafer, with the most extreme devices nearest the edge of the wafer exhibiting peak currents of approximately 10-20% higher than those measured near the center of the 3-inch wafer, as seen in Figure 4.13. The increase of the peak current density near the edge of the wafer is attributable to non-uniformity of the beam flux in the MBE growth system. Since the flux is slightly lower near the edge of the wafers relative to the center, the epitaxial layers are slightly thinner near the edge of the wafer. Because the RTD peak current density is exceptionally sensitive to the barrier thickness, as discussed in Section 2.1, a relative flux decrease of only 1-2% near the edge of the wafer will cause a measurable increase in the RTD peak current. In the case of Wafer 4243, for example, the increase in peak current density of 20% from the center to the edge of the wafer can be explained by difference in barrier thickness of only 1 Å.

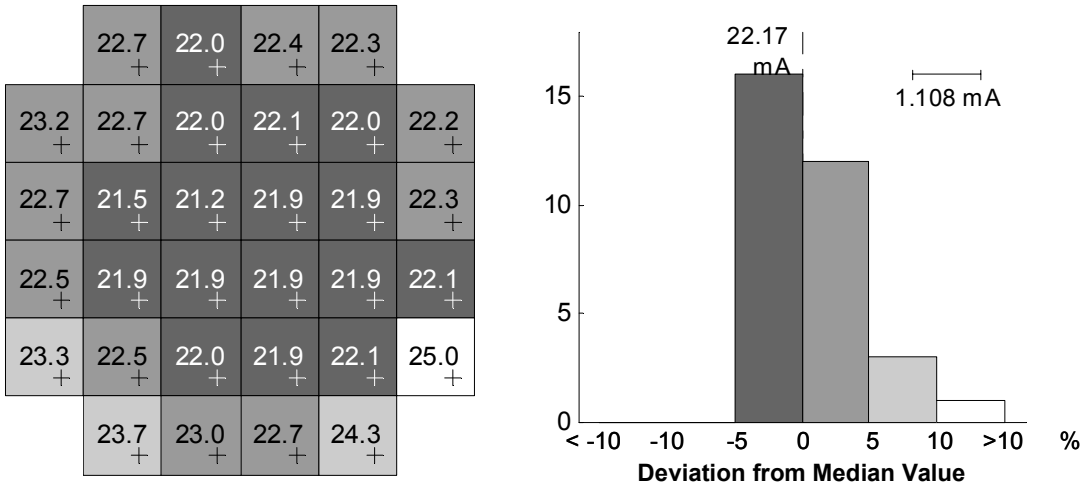


Figure 4.13. Wafer map and histogram of the RTD peak current for a device with area $6 \times 6\ \mu m^2$.

Finally, we see that the peak current of the finished devices does not scale with the nominal device area, as can be clearly seen in Figure 4.14, which plots the distribution of the nominal peak current density for all RTDs on the wafer. From the measured data, the small area RTDs have a larger current than would be expected if it were assumed that the actual RTD area was identical to the drawn area. The cause of the difference between the lack of ideal scaling evident in this wafer map and the near perfect current-area scaling shown in Figure 4.9 from a different wafer after RTD mesa etching is not understood. If the trend were reversed, i.e. the nominal current density decreased as the drawn area, then the likely explanation would be undercut of the etch mask during the wet chemical clean-up etch after forming the RTD mesas. Since the intrinsic current density should be independent of the true device area, there are two potential explanations. First, a sidewall leakage component to the RTD current would be proportional to the perimeter-to-area ratio of the RTD mesa, which is inversely proportional to the RTD width. A sidewall leakage component to the RTD current would also similarly cause an equal or greater increase the valley current, however, which would measurably lower the PVCR for a device with a sidewall leakage current. The corresponding PVCR distribution for the RTDs from Wafer 4243 shown in Figure 4.15 does not support this hypothesis, with no indication of a decrease in PVCR with decreasing device area. Second, the increase in nominal peak current density with decreasing device size could be explained by an increase in actual device area over the drawn area. If the mask dimensions are increased by a constant bias factor in all directions, then the scaling effect is the opposite of mask undercut, and relative increase in device area will be larger for the smaller RTD dimensions. The cause for this increase

in mask area would be inadequate control of the photolithographic process, specifically in either the optical pattern exposure or photoresist development.

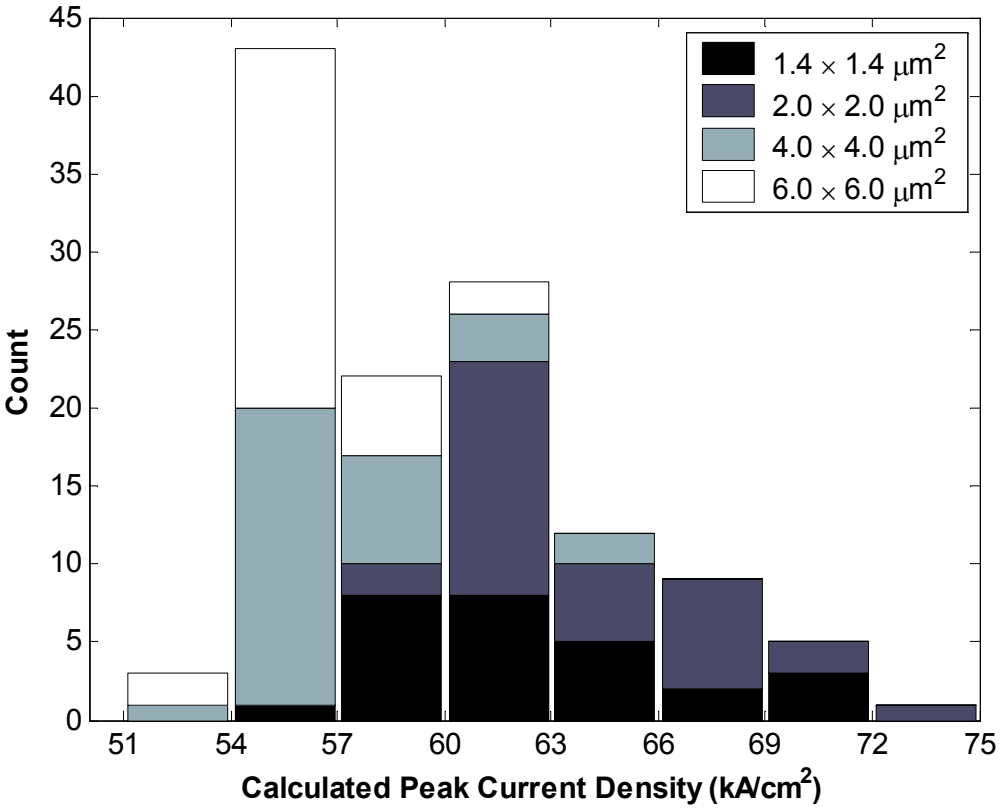


Figure 4.14. Distribution of the peak current density calculated from the drawn RTD areas.

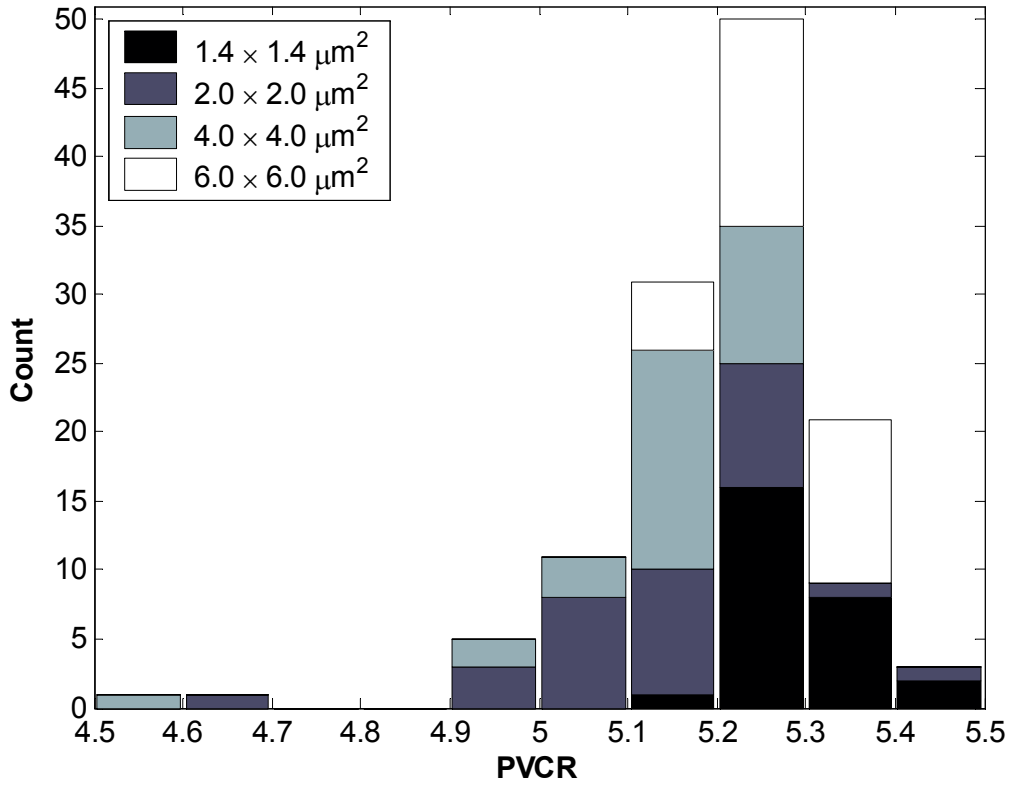
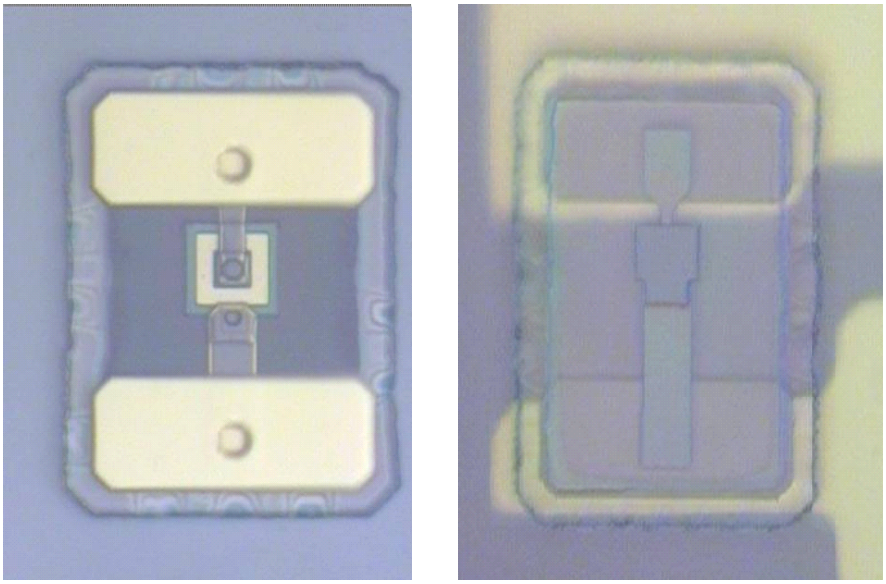


Figure 4.15. Distribution of the measured peak-to-valley current ratio.

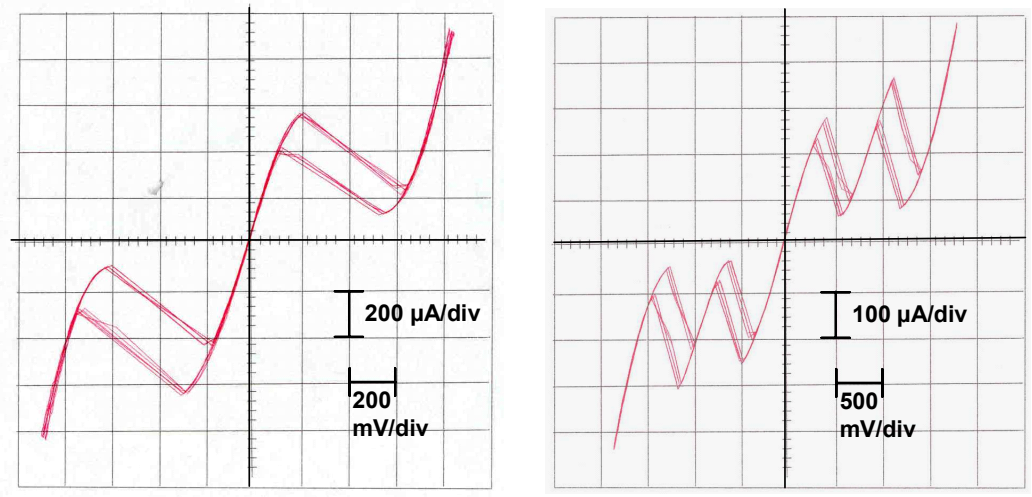
4.3.10. Substrate removal and bonding

A die of the next generation low parasitic RTDs were separated from the InP growth substrate, transferred to pads on silicon using the alignable transfer process mentioned earlier, and detailed in the preceding section. A photomicrograph of the thin-film structure before and after substrate removal and transfer is shown in Figure 4.16. The SOG was undercut by about 5 μm on each side on this particular RTD wafer as a result of overetching the top TiW layer off of the gold. Current-voltage characteristics as measured on a curve tracer are shown after thin-film integration for a single RTD and a series RTD pair in Figure 4.17.



(a) (b)

Figure 4.16 (a) A front-side-only contacted RTD on InP. (b) A front-side contacted thin-film RTD transferred to Ti/Au pads on silicon.



(a) (b)

Figure 4.17 (a) DC trace of a thin-film next generation RTD structure transferred to silicon. (b) DC trace of a series connected RTD pair.

CHAPTER 5

QUANTUM MMIC

5.1. Introduction

In high frequency RF applications, monolithic compound semiconductor integrated circuits have historically held an advantage over silicon on account of the higher speed, lower noise, and greater power efficiency achievable due to the higher electron mobility and velocity. In addition, many RF applications require a semi-insulating substrate such as GaAs, InP, or SiC to allow for high-Q inductors and transmission lines as well as to minimize signal interference due to inadequate substrate isolation. As referenced in Chapter 1, monolithic RTD-HEMT technology has been developed to produce novel analog-to-digital converters, digital logic, and memory circuits with improved functional density. Less progress has been made in the development of monolithic tunnel diode-transistor technologies for analog high-frequency applications.

The Quantum MMIC (monolithic microwave integrated circuit) technology has been developed at Motorola Labs which co-integrates $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ HEMTs with heterojunction interband tunneling diodes (HITDs), grown by MBE on lattice-matched semi-insulating InP substrates [54], [55]. The technology allows for flexibility in meeting the range of matching and power requirements needed for RF applications by varying the doping profiles and, in some cases, the quantum well widths of the HITDs. The HITD layers are vertically stacked on top of the HEMT layers, which are then fabricated with conventional optical lithography and InP-based processing

methods. The measured cutoff frequency of the 0.8 μm HEMT and 2.5 × 2.5 μm HITD were 20 GHz (f_τ) and 13 GHz, respectively. Once the active devices are fabricated, the process is completed with two metal layers and MIM capacitors. No back side processing was performed on the samples in this work.

While InP-based RTDs can offer a higher combination of PVCR and current density, in analog applications the PVCR is not of itself important. Rather, the available peak current, i.e., the difference between the peak and valley currents, and the speed index of the tunneling diode are the relevant figures of merit. HITDs are attractive for RF applications because they can offer high peak current density with an NDR region that spans a wider voltage range than is typically achieved in an RTD due to the latter's narrow resonances. The maximum power output of an NDR diode is given by

$$P = \frac{3}{16}\Delta V \Delta I \,, \tag{5.1}$$

where ΔV and ΔI are the voltage and current span of the NDR region of the diode [56].

5.2. HITD Device Characterization and Modeling

An example of the type of HITD used in this work is shown the epitaxial layer structure of Table 5.1. This type of HITD is a mixed Esaki tunneling diode, which combines the high tunneling current density possible in the narrow bandgap $In_{0.53}Ga_{0.47}As$ (E_g = 0.74 eV) with the larger thermionic emission barrier provided by $In_{0.52}Al_{0.48}As$ (E_g = 1.45 eV) to yield an Esaki diode with improved PVCR. The specific devices characterized in this work incorporate a 20 Å not-intentionally-doped $In_{0.53}Ga_{0.47}As$ layer between the n^+-$In_{0.53}Ga_{0.47}As$ and the p^+-$In_{0.52}Al_{0.48}As$ to reduce the

junction capacitance, at the cost of lowering the peak current density to 18 kA/cm^2. The corresponding band diagrams and J-V characteristic are shown in Figure 5.1 [57].

Table 5.1 Epitaxial layer structure of InP-based mixed Esaki tunneling diode

	Composition	Thickness (Å)	Doping
4	$In_{0.53}Ga_{0.47}As$	500	C p^{++}
3	$In_{0.52}Al_{0.48}As$	500	Si p^{++}
2	$In_{0.53}Ga_{0.47}As$	1000	Si n^{+}
1	$In_{0.52}Al_{0.48}As$	5000	
0	InP substrate		

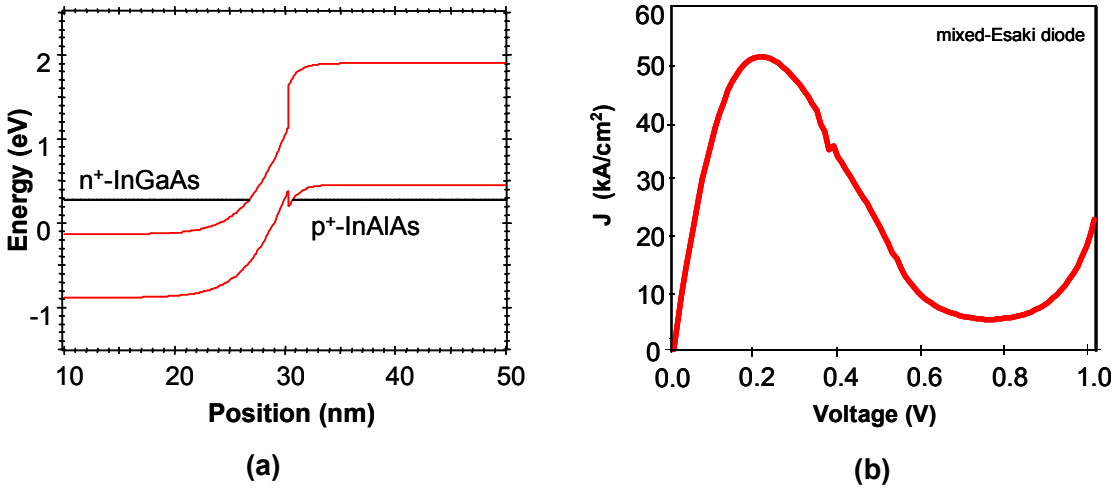


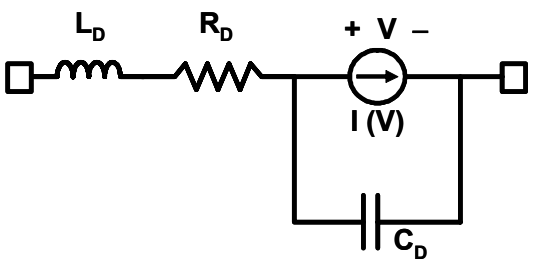
Figure 5.1 (a) Energy band diagram of the mixed-Esaki $In_{.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ tunnel diode described in Table 5.1, with (b) the corresponding J-V characteristic.

Accurate modeling of the HITD and HEMT are essential in the design of the oscillators and amplifiers. For the HEMT model, a linear hybrid-π model was employed with parameters fitted from s-parameter measurements up to 10 GHz. To accurately model the HITD, an equation based model [58] was used using DC measurements to characterize the HITD's nonlinearity, and low frequency RF impedance measurements to

determine the diode capacitance and inductance. The HITD model is schematically illustrated in Figure 5.2, with the equation based nonlinear voltage-controlled current source governed by the polynomial

$$I(V) = g_1 V + g_2 V^2 + g_3 V^3 + g_4 V^4 + g_5 V^5, \qquad (5.2)$$

where the coefficients $g_1, \ldots, g_5$, are determined from device measurements. The model parameters used in design for a $2.5 \times 2.5\ \mu m^2$ HITD are tabulated in the inset of Figure 5.2.

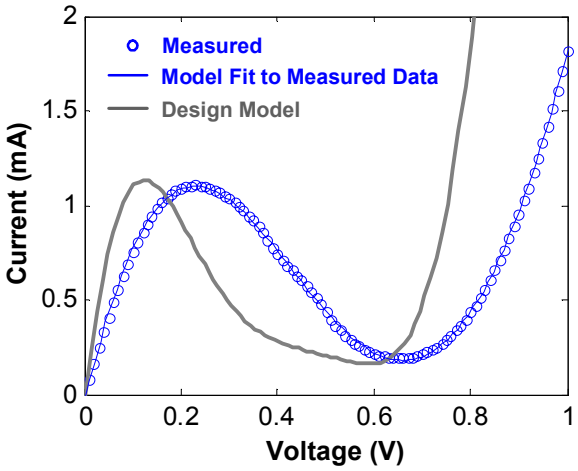


$$I(V) = g_1 V + g_2 V^2 + g_3 V^3 + g_4 V^4 + g_5 V^5$$

Parameter	Value
L_D	0.2 nH
C_D	82 fF
R_D	12 Ω
g_1	0.02542
g_2	- 0.1905
g_3	0.5591
g_4	- .7423
g_5	0.372

Figure 5.2 The HITD large signal model used for design simulation for a $2.5 \times 2.5\ \mu m^2$ mixed-Esaki type HITD.

It should be noted that the simple fifth order polynomial nonlinear current model is only useful as a circuit simulation tool. Slight changes in the diode I-V can produce large shifts in the individual polynomial coefficients, and the individual coefficients can't be easily linked to the device structure as they can in a physics-based model. Nevertheless, the polynomial model has the advantages of offering excellent agreement to the measured I-V data as shown in Figure 5.3 in addition to excellent computational speed and numerical stability.



(a)

Parameter	Design Values	Measured Values
R_D	12 Ω	12 Ω
g_1	0.02542	0.01257
g_2	- 0.1905	- 0.04303
g_3	0.5591	0.04892
g_4	- 0.7423	- 0.002062
g_5	0.372	0.004259

(b)

Figure 5.3 (a) The measured and modeled diode I-V characteristics compared with that used in design. (b) The corresponding parameters for the nonlinear current sources in the model.

5.3. HITD Oscillator

Using the above described HITD model, a 5 GHz C-band oscillator was designed, as shown in Figure 5.4 [59]. The oscillator has only one power supply, the diode bias, and is designed for a 50 Ω load. Since there are no transistors in this design the circuit area was made very small, with the layout area limited by the capacitors, inductors and probe pads. Due to the single HITD design, the power output was only -19.0 dBm at 4.686 GHz, but this number is not unreasonable relative to the low DC power consumption of 0.32 mW. The lower than designed oscillation frequency is a result of the actual specific MIM capacitance being higher than the design specification. The frequency spectrum of the oscillator was measured with an Agilent 8565E spectrum analyzer. The harmonics and fundamental peak spectrum are shown in Figure 5.5.

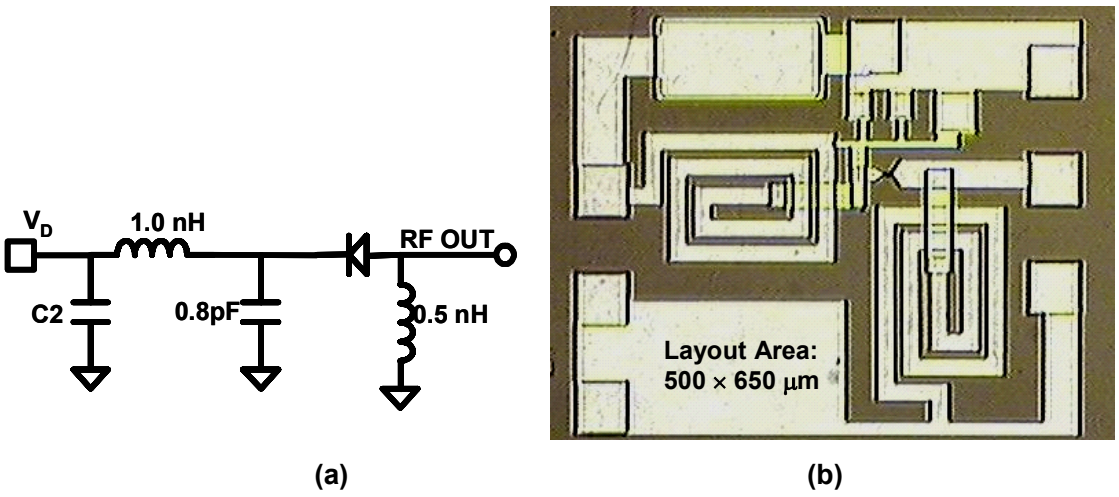


Figure 5.4 (a) The HITD C-band oscillator circuit schematic, and (b) chip layout.

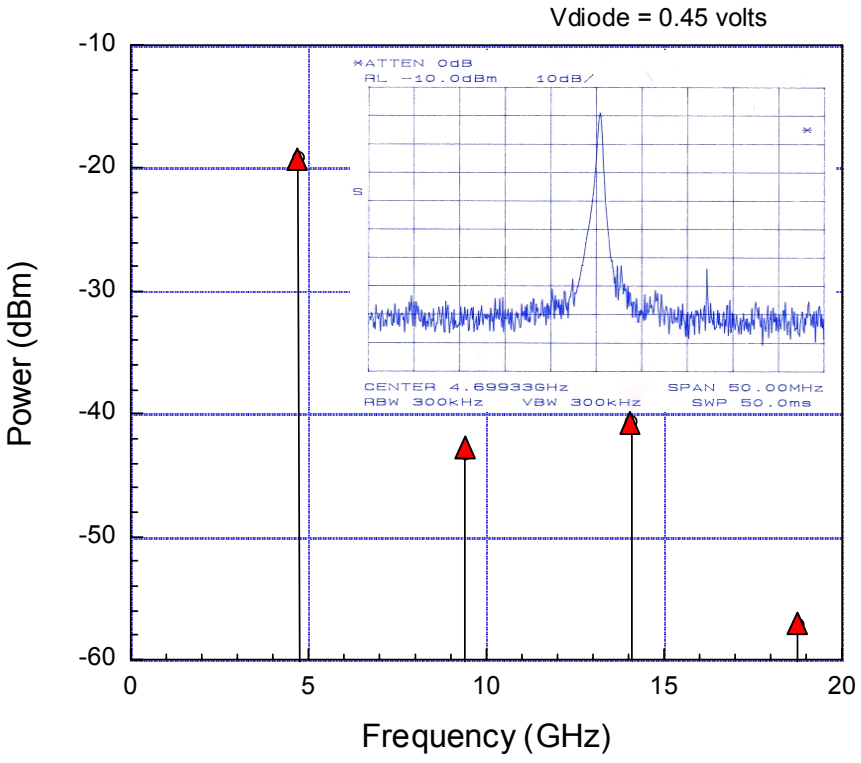


Figure 5.5 The harmonics of the C-band HITD oscillator, with the fundamental peak spectrum shown in the inset.

5.4. Low Noise Amplifiers

NDR devices can also be used as amplifiers. Amplification by a negative resistance is analogous to more intuitive attenuation by a positive differential resistor. More interestingly, tunnel diodes have been proposed for application in low-noise amplifiers because they may be able to provide gain with very low noise figures when combined with transistors due to the quantum tunneling nature of the electron transport.[60], [61]. Using this principle, an LNA was designed by Sangwoo Han, as shown in Figure 5.6. A 12.5 × 2.5 μm HITD is used at the input. The single stage LNA was designed for 6 GHz operation and 50 ohm source and load impedances. Unfortunately, measurements were disappointing; the circuit oscillated under all bias conditions in which the HITD was in the NDR region, illustrating the inherent difficulty of designing circuits with devices that have NDR over the entire frequency span from DC to its cutoff frequency.

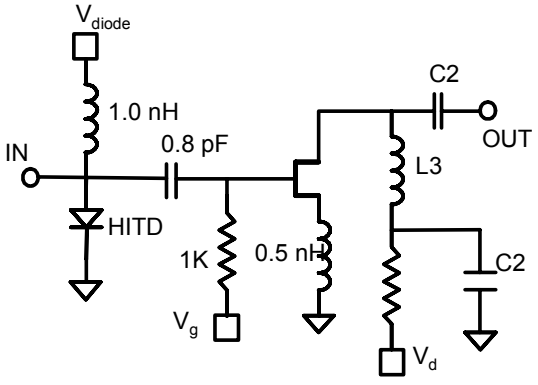


Figure 5.6 Circuit schematic of the C-band HITD LNA.

5.5. HITD-FET (HITFET) RF Noise Characterization

5.5.1. Experimental method

In order to characterize the RF noise properties of a combined HITD-FET (HITFET), a representative 4 × 100 μm HITFET was characterized using an ATN noise parameter measurement system from 2 to 8 GHz. In order to compare the HITFET noise characteristics to that of an identical HEMT without the HITD, the 2.5 × 2.5 μm HITD was severed from the input with a manual laser scribe, allowing the HEMT alone to be tested, as shown in Figure 5.7.

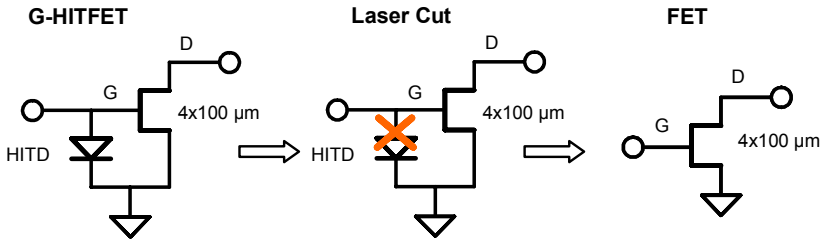


Figure 5.7 The G-HITFET with the HITD severed from the input to allow testing of the FET alone.

5.5.2. Results

The DC output characteristics of the HITFET and FET are shown in Figure 5.8. From the DC input characteristics shown in Figure 5.9(a), it is evident that the G-HITFET is unstable over most of its NDR region, which is problematic in terms of acquiring a reliable noise figure measurement. For this reason, the HITFET and FET were characterized at input biases of −0.45 V and−0.65 V. At −0.45 V, the HITD is near maximum negative differential conductance, but also maximum instability. At −0.65 V,

the HITD has much lower negative differential conductance, but is stable when biased through the 50 Ω network analyzer inputs. The I-V characteristics of the HITD at the input as well as the gate leakage of the FET after severing the HITD are shown in Figure 5.10.

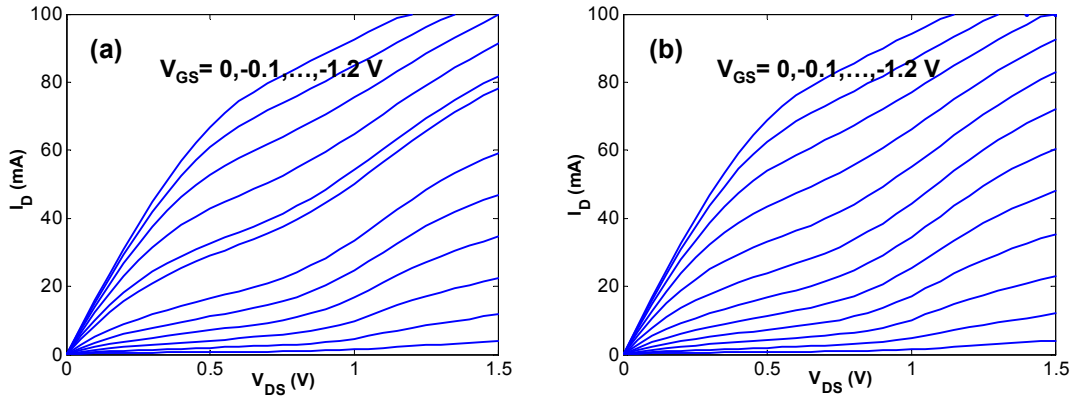


Figure 5.8 DC output characteristics of the (a) G-HIFET and (b) FET after the HITD was severed.

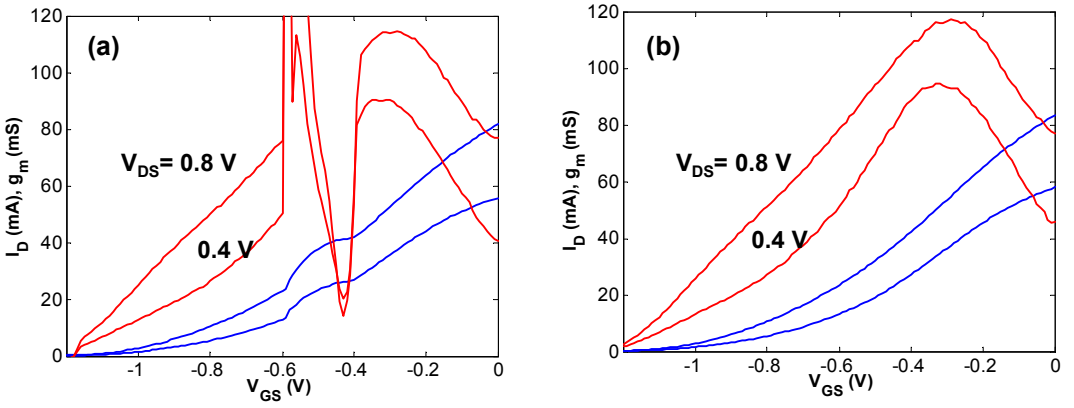


Figure 5.9 DC input characteristics of the (a) G-HIFET and (b) FET after the HITD was severed.

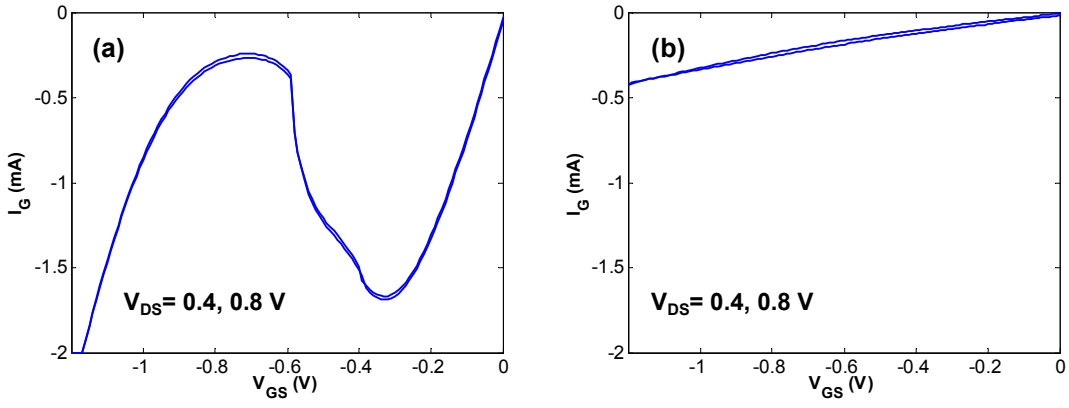


Figure 5.10 DC gate leakage characteristics of the (a) G-HIFET and (b) FET after the HITD was severed.

S-parameter measurements did not show signs of instability, and there was very little observed difference between the RF characteristics before and after severing the HITD. The only observed difference was a slight shift in s_{11} due to the presence of the NDR of the HITD on the HITFET input, seen in Figure 5.11. There were no signs of self-oscillation during the s-parameter measurements, at either bias point. The RF noise measurements, on the other hand, showed clear signs of self-oscillation when the source impedance was swept using solid-state tuners. This was not unexpected, since the HITFET would be expected to have a more limited region of stability with respect to the source impedance. For this reason, a determination of the true noise parameters (F_{min}, R_n, and Γ_{opt}) was not possible. Since the devices did not appear to oscillate during the 2-port s-parameter measurements with a 50 ohm source impedance, the only useful parameter that could be compared was NF_{50}, the device noise figure near 50 ohm source impedance.

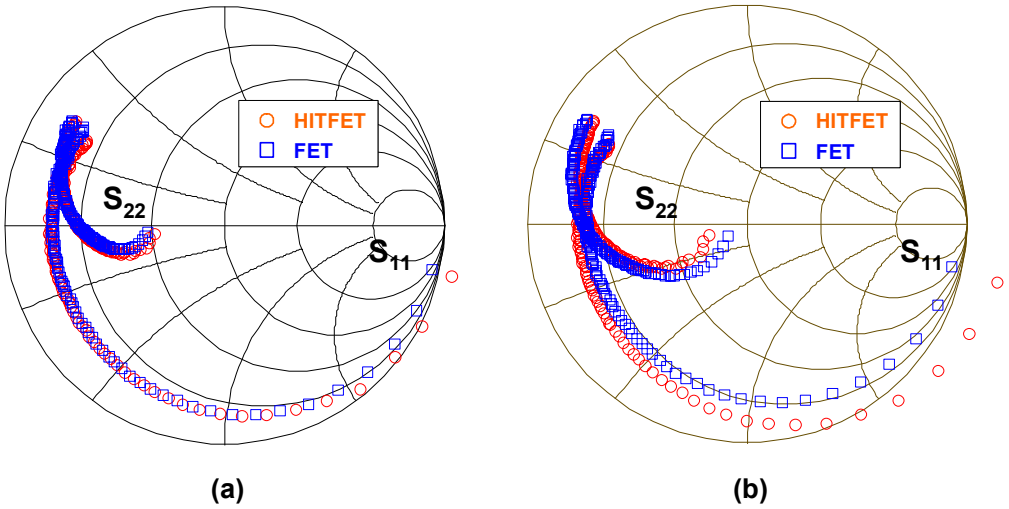


Figure 5.11 (a) The measured s-parameters from 0.25 to 26.5 GHz for the HITFET and the FET after the HITD was severed at V_{gs}= −0.45 V. (b) The measured s-parameters at V_{gs}= −0.65 V.

The measured 50 Ω noise figure is shown in Figure 5.12 for a bias of $V_{gs} = -0.45$ V and $V_{gs} = -0.65$ V. The drain-source voltage is 0.8 V in both cases. Clearly, much of the HITFET noise data is unreliable, even at $V_{gs} = -0.65$ V, where there is less negative conductance. This is probably a result of the noise source and PIN diodes in the source tuner causing internal oscillations in the test system when coupled to the HITFET input. As such, it is uncertain as to whether the HITFET offers superior noise figure. The FET noise figure shows conventional frequency dependence for a FET operating well below its f_τ. There is considerable excess noise, about 5 dB at −0.45 V gate bias, and 6 dB at −0.65 V gate bias, which is attributable to the relatively high gate leakage currents. The monotonic increase in noise figure with respect to frequency results from thermal noise sources in the HEMT.

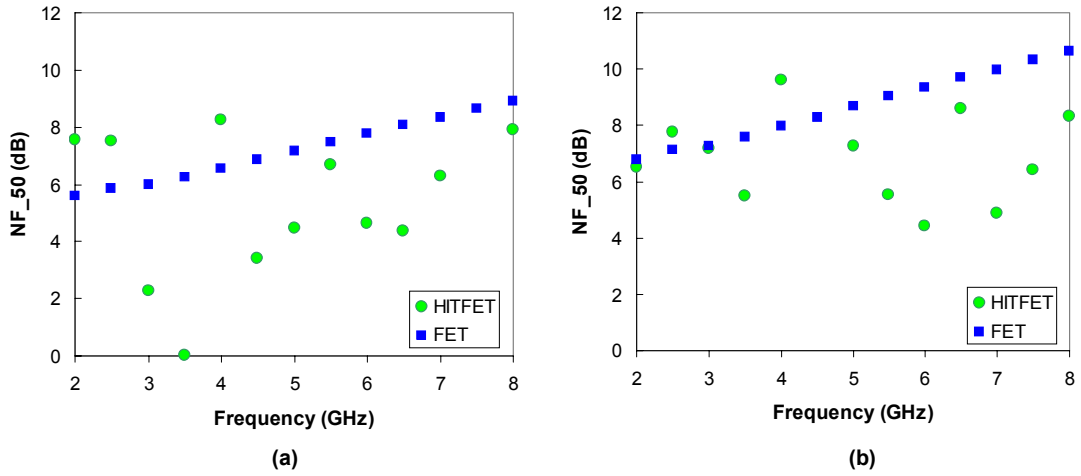


Figure 5.12 Measured noise figure in a 50 Ω environment for the HITFET and FET measured at a gate bias of (a) −0.45 V and (b) −0.65 V

5.5.3. Conclusions

Given the above mentioned experience with the challenges of stabilizing an integrated NDR device, it seems reasonable to question the wisdom of applying tunnel diodes in low-noise amplifiers. First, the assumption that the tunnel diode would not add microwave noise to the transistor is very optimistic. The LNA design was purely investigational, and was attempted with the reasoning that the HITD's negative resistance would cancel much of the FET's input gate resistance, thereby lowering the noise figure. This was a rather naïve assumption, since the thermal noise source presented by the FET gate will still be present, and the HITD in parallel with the gate should only serve to shift the source impedance presented to the FET. At a minimum, there will be an added $\sqrt{2qI}$ shot noise component added to the transistor noise at the input that should result in an undesirable excess noise in microwave amplifiers. Given the difficulty of stabilizing NDR devices combined with the small amount of additional gain available, tunnel diodes

have doubtful utility in microwave amplifiers, and to date no such amplifiers with this topology have been reported.

CHAPTER 6

DEVELOPMENT OF THE InAs/AlSb HEMT FOR LOW-POWER MMICS

6.1. InAs/AlSb HEMT Electron Transport Properties and MBE Growth

The InAs/AlSb HEMT, like its counterparts in the GaAs and InP material systems, derives its high speed performance from the inherently fast electron transport properties of the channel semiconductor, as opposed to the modern silicon FETs for which advanced device engineering dictates the transistor performance. As was discussed in Chapter 1, the low effective mass of InAs ($m_e = 0.023m_o$) permits the realization of InAs quantum wells with very high electron mobilities. Since the nearly lattice-matched AlSb has a conduction band offset of 1.35 eV relative to InAs [62], the InAs/AlSb quantum well can hold a much higher electron density than a GaAs/AlGaAs or InGaAs/InAlAs HEMT. The inherent improvement in electron transport properties in the InAs/AlSb HEMT as opposed those of the GaAs or InP-based HEMT were already illustrated in the compiled Hall data in Figure 1.3. The typical InAs/AlSb HEMT exhibits a room temperature mobility of about 18,000 cm^2/Vs at a sheet charge density of $3\text{-}4 \times 10^{12}$ cm^{-2}, as compared with 6,000 and 10,000 cm^2/Vs for top quality GaAs and InP-based HEMTs, respectively.

As mentioned in Chapter 1, in order to produce MMICs, a semi-insulating substrate is required in order to avoid excessive substrate loss and RF coupling through the substrate. Due to the lack of a stable semi-insulating substrate that is lattice-matched to InAs, the HEMT structures are metamorphic HEMTs (MHEMTs) grown on readily available 4-inch semi-insulating GaAs substrates, using a 1-2 μm metamorphic buffer to

reduce the initial threading dislocation density from approximately 10^{10} cm^{-2} to 10^{8} cm^{-2}. The particulars of the MBE growth sequence such as the nucleation and AlSb buffer layer sequences were based on those developed in the late 1980s and early 1990s by H. Kroemer's group at UCSB [63].

The HEMT starting material was grown by MBE on a semi-insulating GaAs substrate, using a 2 μm AlSb metamorphic buffer to accommodate the approximately 7% lattice mismatch. The HEMT active layers were grown at 500 °C over a 2000 Å $Al_{0.8}Ga_{0.2}Sb$ stabilizing buffer, which was needed because pure AlSb is unstable in air. The 80 Å AlSb lower barrier was followed by a 125 Å InAs channel, with the interface between the layers forced to be InSb-like in order to achieve the best possible electron mobilities [64], [65]. The InAs channel was followed by a 130 Å upper AlSb barrier which includes a delta-doping plane of approximately 4×10^{12} cm^{-2} Te density. Finally, the HEMT was capped with a 50 Å strained $In_{0.5}Al_{0.5}As$ layer, which serves to provide a chemically stable surface as well as to lower the gate leakage current relative to a comparable HEMT with a GaSb cap [66]. The energy band diagram and epitaxial layer structure of the HEMT is shown in Figure 6.1. Hall measurements determined the electron sheet concentration and mobility of the as-grown material to be 3.7×10^{12} cm^{-2} and 19,000 cm^2/Vs at 295 K, respectively. The corresponding values at 77 K were 3.4×10^{12} cm^{-2} and 65,000 cm^2/Vs, which indicate excellent material quality for an InAs/AlSb HEMT with AlSb buffers at this level of doping.

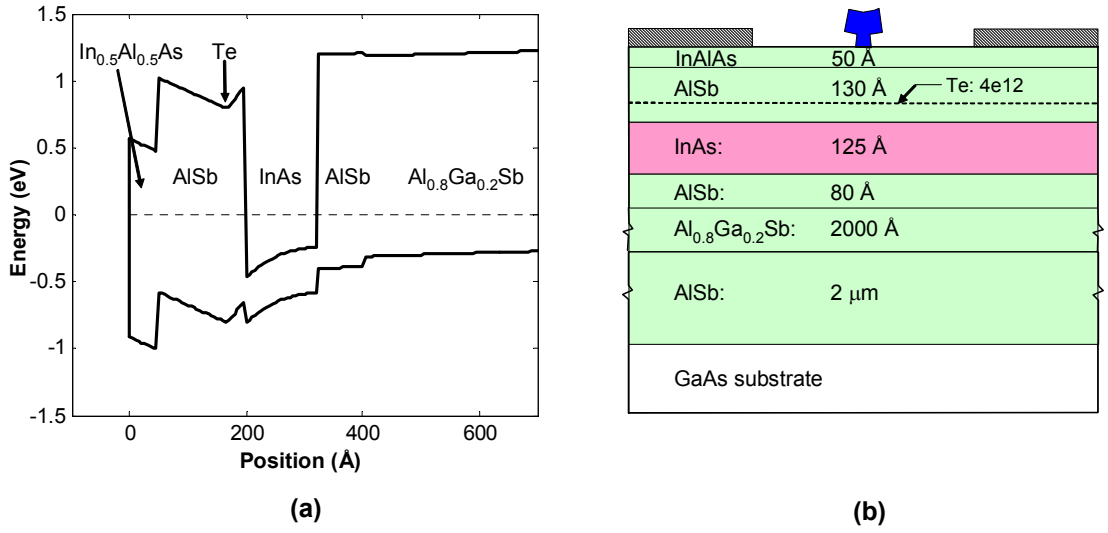


Figure 6.1 (a) Energy band diagram of the InAs/AlSb HEMT. (b) The epitaxial layer structure of the InAs/AlSb HEMT.

6.2. Overview of the InAs/AlSb HEMT MMIC Process

From the beginning of the project, the goal has been to transition the InAs/AlSb HEMT from laboratory demonstration to MMIC technology. For this reason, the InAs/AlSb HEMT epitaxial layer design and process were tailored to be integrated circuit compatible. InAs/AlSb MMIC process flow outlined in Figure 6.2 achieves this goal by leveraging existing GaAs MMIC production processes in the fabrication of InAs/AlSb integrated circuits on GaAs substrates. While the InAs/AlSb HEMT formation is fundamentally different from that of a GaAs HEMT, the process steps following the active device formation, i.e. from first metal onward, are nearly identical to those used in the GaAs HEMT MMIC process.

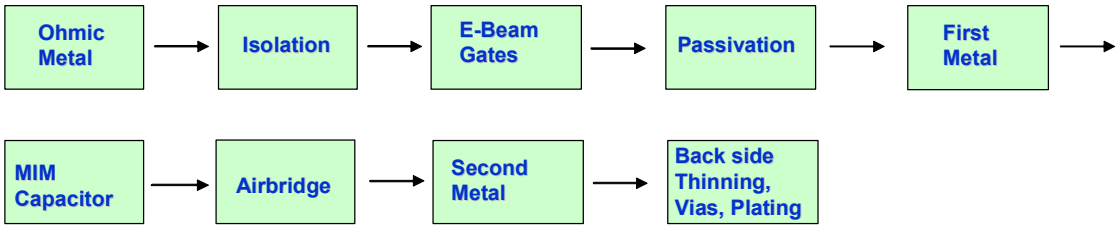


Figure 6.2 Summary of the InAs/AlSb HEMT MMIC process.

The HEMT process steps are detailed in Section 6.4, but a brief summary of the generic MMIC process is provided here. The HEMT is fabricated using a conventional mesa process, by wet chemical etching past the InAs channel to the $Al_{0.8}Ga_{0.2}Sb$ stable buffer layer. Ohmic source and drain contacts are deposited using e-beam evaporation, followed by patterning and lift-off of submicron gates with electron beam lithography. The device is immediately coated with PECVD SiN_x to serve as passivation and device protection. Metal1 is evaporated and lifted off, and a second PECVD SiN_x layer is deposited to serve as the capacitor dielectric. Air bridge patterning and second metal deposition complete the front side MMIC process (Figure 6.3(a)). To allow for microstrip transmission lines and low-inductance common ground access, the GaAs substrate is thinned and polished to 3 mils. Thru-vias are etched by RIE, and a gold back side ground plane is plated. Finally, streets are patterned and etched in the back side metal to facilitate the scribe and break of the wafer into discrete chips. All mask steps except for the gates are patterned with conventional optical lithography. A schematic of the InAs/AlSb MMIC with capacitors, microstrip lines, epitaxial resistors, and thru-vias is shown in Figure 6.3(b).

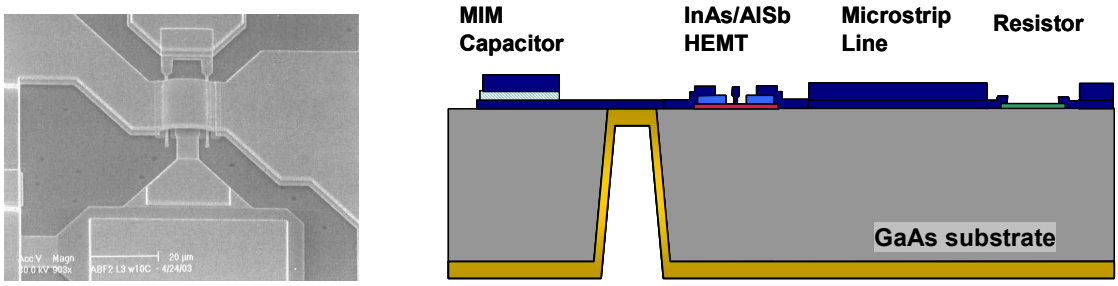


Figure 6.3 (a) SEM image of a 2 × 20 μm InAs/AlSb HEMT with air bridges. (b) Schematic of a GaAs MMIC.

6.3. Early Challenges

The first attempts at fabricating InAs/AlSb HEMTs were frustrating. The ultimate successful HEMT process was only developed after many unsuccessful attempts which led to the refinement of both the fabrication process and the epitaxial design and growth procedure. Two of the major challenges and their resolutions follow in this section: the absence of a mature knowledge base in antimonide semiconductor processing and micro-cracks.

6.3.1. Antimonide semiconductor processing difficulties

One of the major obstacles in the development of InAs/AlSb MMICs is the lack of experience in antimonide processing relative to the decades of processing experience in GaAs and InP-based semiconductors. The first problem to be dealt with was the extreme reactivity of the AlSb in air. If, for example, the AlSb metamorphic buffer layer was exposed, it would immediately oxidize, and within one day would be oxidized all the way to the GaAs substrate. Since the AlSb roughly doubles in volume as it oxidizes, the entire epitaxial layer would then crack and flake as shown in Figure 6.4, destroying the

wafer completely. This problem was only solved by expanding the thickness of the $Al_{0.8}Ga_{0.2}Sb$ stabilizing buffer layer from 300 Å to 2000 Å to allow for a safe margin for etching the active device mesas.

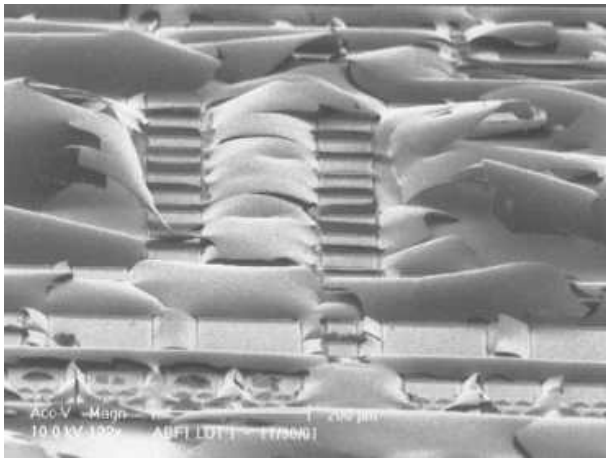


Figure 6.4. SEM micrograph of an InAs/AlSb HEMT wafer after the AlSb buffer oxidized and cracked.

In addition to the oxidation problems associated with the AlSb buffers, the early HEMTs employed a 50 Å GaSb cap layer instead of the $In_{0.5}Al_{0.5}As$ layer as shown in Figure 6.1(b), which created multiple difficulties in the HEMT processing. First, GaSb (and AlSb) were etched in the tetramethyl ammonium hydroxide (TMAH) photoresist developers. Although the etching was slow, about 1 Å/sec, this precluded the possibility of rework after photolithography. Second, it was not possible to achieve acceptable ohmic contact resistances with GaSb-capped HEMTs. Alloyed Pd and AuGe-based ohmic contacts were unable to produce contacts with resistances below 0.3 Ω-mm, and the contacts exhibited poor linearity and reproducibility. An ohmic contact process by which the InAs channel was directly contacted after etching the overlying cap and

barriers was tried without success. The first such experiments used NH_4OH: H_2O and CH_3COOH: H_2O_2: H_2O as selective wet chemical etches between Al(Ga)Sb and InAs [67], and yielded very poor contacts, with unacceptable contact linearity and contact resistances over 0.5 Ω-mm. The poor contacts could be explained by the either the presence of a residual Sb oxide layer between the ohmic metal and InAs or by the exposed InAs channel in the laterally undercut region. One experiment that addressed these problems used a BCl_3 RIE to etch the contact holes to the InAs channel in order to minimize the lateral undercut and exposed InAs surface at the edge of the ohmic metal. While the contact resistance improved to 0.2 Ω-mm, this was still not acceptable for a high-speed, low-voltage HEMT technology. When the transition was made to $In_{0.5}Al_{0.5}As$ caps, low-resistance, highly reproducible diffused Pd ohmic contacts were readily obtained. Finally, HEMTs with the GaSb cap showed high gate leakage, likely due to surface conduction between the gate and source/drain ohmics, in addition to hysteretic effects indicative of charge trapping. Again, these effects were eliminated after the transition was made to $In_{0.5}Al_{0.5}As$ caps.

6.3.2. Micro-cracks in the InAs/AlSb HEMT layers

While analyzing the Hall data on as-grown InAs/AlSb HEMT wafers with $In_{0.5}Al_{0.5}As$ caps it became evident that the voltages in the van der Pauw measurement varied substantially depending on the direction of the forced current. The magnitude of the anisotropy was variable, but it was more pronounced at 77 K than at room temperature. Ensuing analysis of TLM data for ohmic contacts on pieces of these wafers confirmed this observation, showing a definite pattern in which the channel sheet

resistance was typically about 15% higher in the [011] orientation relative to the $[01\bar{1}]$ orientation.

Insight as to the cause of this anisotropic degradation of the channel conductivity was provided by atomic force microscopy of the as-grown InAs/AlSb HEMT wafers. Tiny micro-cracks of at least 200 Å in depth were observed on the surface of the wafers with $In_{0.5}Al_{0.5}As$ caps, and these cracks were primarily oriented parallel to the $[01\bar{1}]$ axis. Figure 6.5 shows an example of an AFM scan of such a wafer with a moderate micro-crack density. It is suspected that these micro-cracks degraded the mobility of electrons in the direction perpendicular to the cracks. This hypothesis is supported by the dramatic increase the anisotropy at 77 K relative to that measured at room temperature, implying that the mobility cannot increase with decreasing temperature as the mean free path of the electrons becomes larger than the separation between cracks. The degree of anisotropy was later characterized precisely by including process control monitors on the HEMT masks that allow for four-wire resistor measurements of two ten-square epitaxial resistors oriented along the fundamental crystal axes.

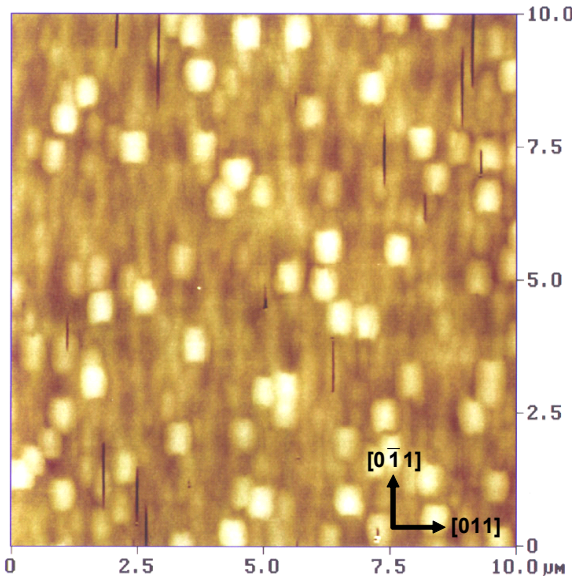


Figure 6.5 Atomic force micrograph of an InAs/AlSb HEMT layer with the strained $In_{0.5}Al_{0.5}As$ cap showing micro-cracks oriented in the $[01\bar{1}]$ crystal axis

Since the anisotropy was first observed in the HEMTs with $In_{0.5}Al_{0.5}As$ caps, it was suspected that the strained cap layers were responsible for the phenomenon. Indeed, an increased V-to-III flux ratio alleviated this problem to a large extent; the micro-crack densities (defined as the area density multiplied by the average crack length) as determined by AFM were reduced by approximately a factor of five. The problem was effectively eliminated altogether when an abnormally long turn-on transient time was discovered in the arsenic beam, and corrected by a modified control sequence for the valve on the arsenic cracker. The correlation between micro-crack density and conductivity anisotropy is exemplified by the three wafers listed in Table 6.1, progressing from a high micro-crack density of 18,000 cm^{-1} to 3,300 cm^{-1} to zero as the MBE growth modifications were put into place. The corresponding relative anisotropy in the sheet resistance of the InAs channel went down from 98% to 18% to zero for the same three

wafers. Figure 6.6 graphically illustrates the anisotropy effect for wafers listed in Table 6.1.

Table 6.1 Correlation between micro-crack density and conductivity anisotropy in the InAs channel

Wafer No.	53	90	143
MBE Growth Modifications	Original baseline	Increased V-to-III flux ratio	Increased V-to-III flux ratio Improved As valve control
Micro-crack Density (cm^{-1})	18,000	3,300	0
Relative R_{sh} Anisotropy	0.983 ± 0.223	0.183 ± 0.032	0.001 ± 0.005

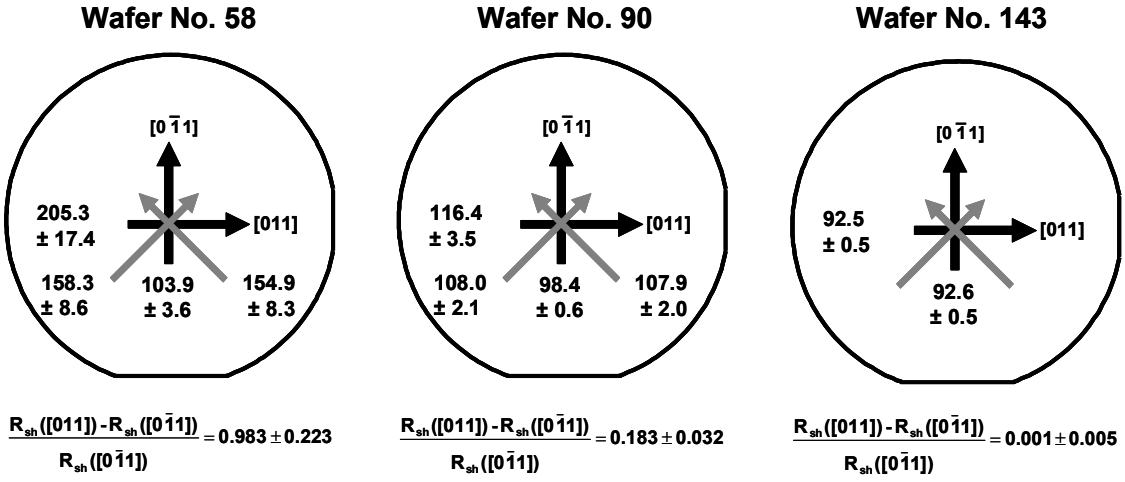


Figure 6.6 The channel sheet resistance in Ω/□ for three InAs/AlSb HEMT wafers with different micro-crack densities.

6.4. The Mature InAs/AlSb HEMT Fabrication Process

While problems besides micro-cracks and the instability of the antimonide semiconductors are still being dealt with on a continuing basis, the fundamental InAs/AlSb HEMT fabrication process has progressed to the point where a reproducible process has been developed. The realization of such a stable process is necessary for MMIC design, for which the designer must have acceptable conformity between the design model and the HEMT that will be realized.

6.4.1. The FET active region: ohmic contacts and mesa isolation

The first two steps in the fabrication of the HEMT are the formation of ohmic contacts and mesa isolation. The realization of low ohmic contact resistances is critical in any high-speed integrated circuit technology, but it is especially critical for a low-voltage, low-noise HEMT technology such as then InAs/AlSb HEMT. The impact of the ohmic contact resistance derives from its contribution to the FET source resistance,

$$R_s = R_c W + R_{sh}\left(L_{gs}/W\right), \tag{6.1}$$

where R_c is the contact end resistance (Ω-mm), R_{sh} is the channel sheet resistance (Ω/□), W is the mesa width, and L_{gs} is the gate-to-source lateral separation. The source resistance causes an approximately proportional decrease in the extrinsic transconductance,

$$g_{me} = \frac{g_{mi}}{1 + g_{mi} R_s}, \tag{6.2}$$

where g_{mi} represents the intrinsic transconductance. It is clear from (6.2) that the higher the intrinsic transconductance, the greater the effect of the contact resistance. For example, the 0.2 Ω-mm ohmic contact resistances obtained on the best process lot for the initial GaSb-capped HEMTs described in Section 6.3.1 would yield a total source resistance of 0.25 Ω-mm for a two-finger HEMT with 0.5 μm spacing between gate and source. Even for a modest intrinsic transconductance of 1 S/mm, the extrinsic transconductance would be reduced by 20%. As a final point, note that the additional source resistance also degrades the minimum noise figure, as is evident in the semi-empirical Fukui equation for minimum noise figure,

$$F_{\min} = 1 + 2k_f \frac{f}{f_\tau} \sqrt{g_m (R_s + R_g)}\,, \tag{6.3}$$

where F_{min} is the minimum noise figure, k_f is a technology dependent fitting parameter, f_τ is the current gain cutoff frequency, and R_g is the gate resistance [68].

The current ohmic contact process employs diffused palladium contacts [69], which have consistently produced ohmic contacts with resistances of under 0.07 Ω-mm. The ohmic metal was patterned with conventional photolithographic techniques and the ohmic metal stack was deposited via electron-beam evaporation. After lift-off of the ohmic metal, the Pd was diffused into the semiconductor with a low temperature anneal at 180 °C for 15 minutes. After mesa isolation, the contact resistances were measured across each wafer using the transfer length method (TLM). The data shown in Figure 6.7 indicate low contact end resistances ranging from 0.04 to 0.07 Ω-mm, with cross-wafer variances of less than 0.02 Ω-mm for the first lot of wafers (1-4), and 0.01 Ω-mm for the subsequent lots (wafers 5-15). The latter number indicates excellent uniformity, considering that the fundamental end resistance measurement repeatability was found to

be about ±0.007 Ω-mm for contact and sheet resistances in this vicinity. There was typically less than 3% cross-wafer variance in the sheet resistance because this parameter should not be process-dependent. The variation in channel sheet resistance from wafer to wafer was almost certainly dominated by deviations in the Te doping level. The specific contact resistances shown in Figure 6.7 were calculated with the transfer length approximation, whereby

$$\rho = \frac{R_c^2}{R_{sh}}, \tag{6.4}$$

and, therefore, the variances of ρ are expected to be larger than those of R_c. The specific contact resistances were in the 2-5 × 10^{-7} Ω-cm^2 range.

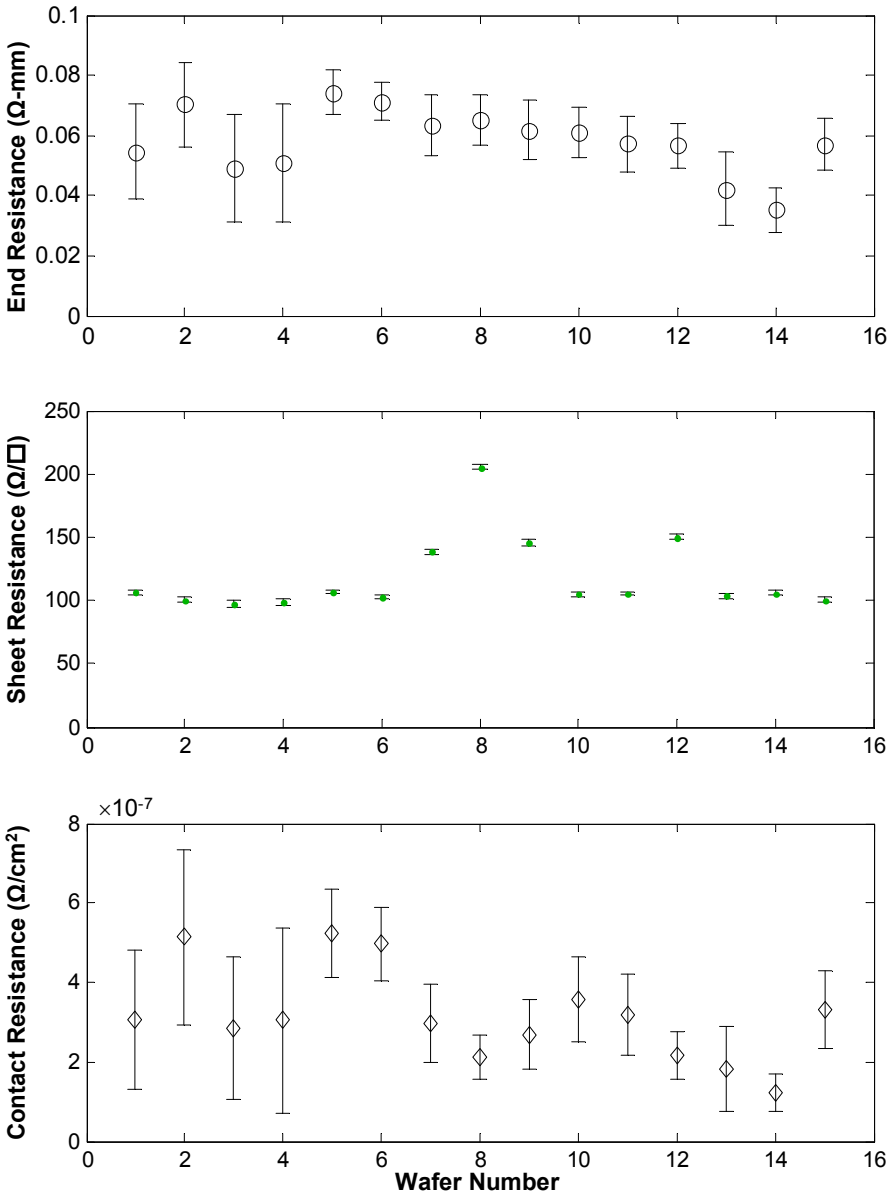


Figure 6.7 The measured ohmic contact resistances for InAs/AlSb HEMTs with the Pd-based diffused ohmic contacts, as determined by the TLM method

The shallow mesa isolation was accomplished through wet chemical etching, using a sequence of the selective wet chemical etchants referenced previously [67], or by a timed non-selective wet etchant. After the isolation etch, a lateral recess etch of the InAs channel was performed with a selective InAs etchant, typically CH_3COOH: H_2O_2: H_2O or citric acid: H_2O_2 in order to prevent the possibility of the gate contacting the channel at the edge of the isolation mesa.

6.4.2. Completing the InAs/AlSb HEMT: gates and passivation

The submicron gates were fabricated with direct write electron beam lithography, using a trilayer PMMA/PMMA-MMA/PMMA resist stack in order to yield T-gates. Gates were written with gate lengths ranging from 0.2-0.3 μm. A Ti/Pt/Au gate was e-beam evaporated and lifted off in acetone. A deposition of 350-500 Å of PECVD SiN_x for passivation and device protection completes the active device fabrication. A nominally 0.2 μm InAs/AlSb HEMT cross-section is pictured in the SEM micrograph of Figure 6.8.

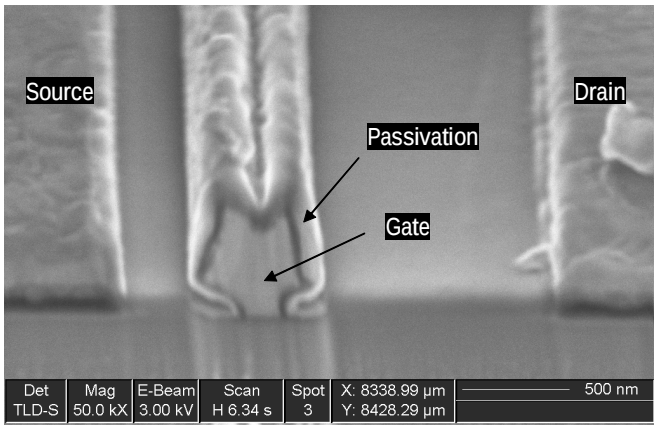


Figure 6.8 Cross-sectional SEM image of an InAs/AlSb HEMT

Following the active device fabrication, the InAs/AlSb HEMT wafers can be run through the baseline GaAs MMIC process described earlier in Figure 6.2, from Metal1 to chip cleaving, with minimal modification. After first metal, probable HEMTs are tested on-wafer in order to inspect yield and evaluate the preliminary device performance. Figure 6.9 shows the results of a wafer map of a 2×20 µm HEMT. The yield was excellent, with 34 of 37 transistors (93%) yielding. It should be noted that the three non-conforming transistors were located on the edge of the field on the side of the wafer where they would be closest to the wafer edge. When the edge die are excluded, the yield was 100%.

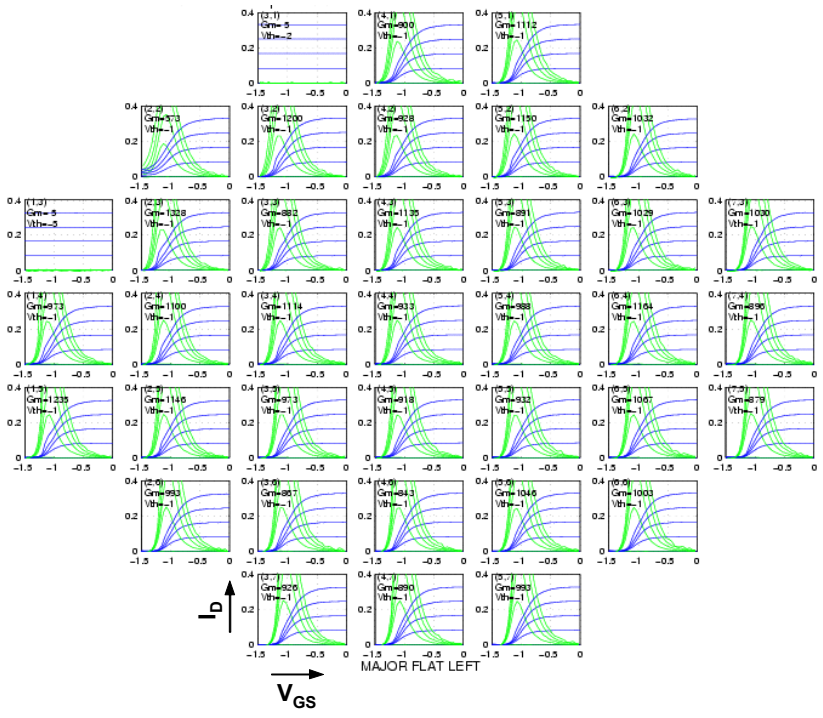


Figure 6.9 Wafer map of the DC input characteristics of a 2×20 µm HEMT

6.5. InAs/AlSb HEMT DC Characteristics

The transistor with a nominal gate length of 0.2 μm has typical DC output characteristics for a doped InAs/AlSb HEMT (Figure 6.10). Holes generated by impact ionization enhance the drain output conductance by forward biasing the source-to-channel barrier, often referred to as the "kink effect" [70]. The on-state soft breakdown voltage is 0.4 V, which is adequate for the ultra-low voltage applications for which the InAs/AlSb is targeted. For a 2 μm source-to-drain spacing, the zero-bias total source-drain access resistance is 0.30 Ω-mm, a value that should be as low as possible to achieve high performance at low drain voltages. There is no "knee" in the drain current at $V_{gs} = 0$, as would be expected in a conventional GaAs or InP-based HEMT, because there is neither saturation of the electron velocity nor pinch off of the channel at the drain bias voltages measured. The channel pinch off voltage is -1.15V.

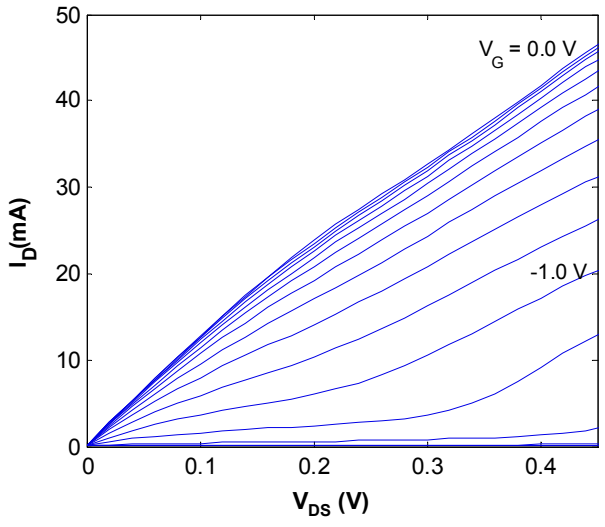


Figure 6.10 The DC output characteristics of a 2 × 20 × 0.2 μm InAs/AlSb HEMT.

Further insight into the transistor's DC operation can be gained from the HEMT's DC input and sub-threshold characteristics. Figure 6.11(a) shows the drain current and DC transconductance as a function of the gate voltage for the same HEMT from Figure 6.10. Impact generated holes also enhance the DC transconductance, with the DC g_m increasing significantly as the *drain* voltage is increased, as indicated by the peak g_m of 1.5 and 2.1 S/mm at drain voltages of 0.3 V and 0.4 V, respectively. The large values for the DC g_m are primarily artifacts of the rise in output conductance caused by the kink effect, and as such these large peak DC transconductance numbers would not translate into a correspondingly large power gain.

In the sub-threshold characteristics of Figure 6.11(b), the classic sign of impact ionization is clearly seen in the gate current: a non-monotonic (with respect to V_{gs}), bell-shaped gate leakage current. Conventional gate leakage due to thermionic or thermionic-field emission electrons past the barrier always increases with increasing negative gate bias, but the signature of impact ionization is an excess gate current attributable to impact-generated holes being collected by the negatively biased gate. Before delving further into the role of impact ionization on the device's DC characteristics, it is should be noted that the gate diode characteristics ($V_{ds} = 0$ V) of the device show very low leakage currents, comparable to the best published results [71].

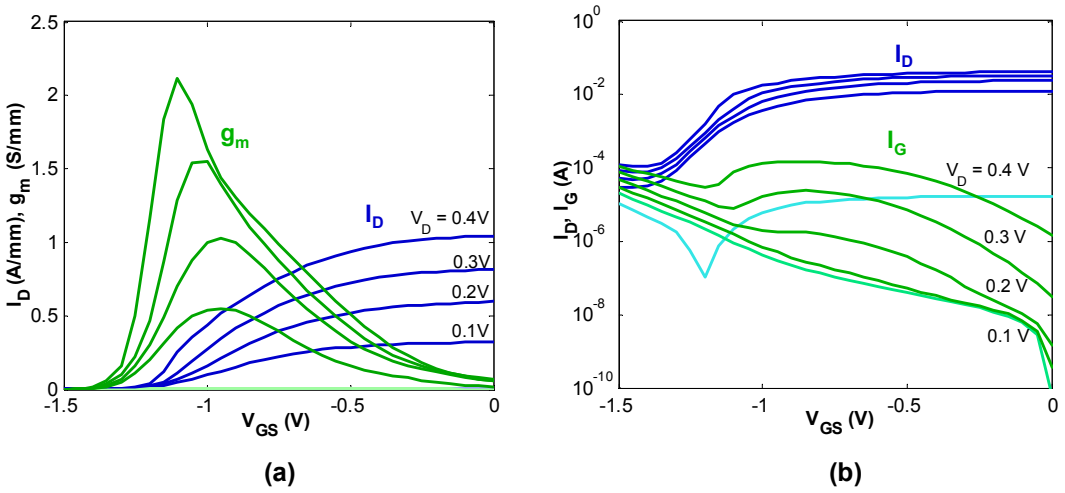


Figure 6.11 (a) HEMT drain current and DC transconductance g_m for a $2 \times 20 \times 0.2$ µm InAs. (b) Subthreshold characteristics of the same transistor.

The mechanics of the kink effect can be understood by referring to the band profile from the source to drain region in the InAs channel, illustrated in Figure 6.12(a). When an electron moving in the InAs channel towards the drain, it gains energy as it enters the high field space charge region between the gate and drain. When the hot electron's energy is comparable to the band gap of the channel (0.36 eV), it can undergo impact ionization, generating an electron-hole pair. The impact-generated hole will drift back towards the source. Besides recombining with an electron, the hole can either collect at the gate-source barrier or be swept into the gate. The latter effect is more pronounced in the InAs/AlSb HEMT than in an $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ HEMT due to the absence of a valence band barrier on account of the staggered band lineup between InAs and AlSb, seen in Figure 6.12(b). This explains the near exponential increase in the gate leakage current at drain bias voltages above 0.2 V seen in Figure 6.11(b). The gate leakage current increases as V_{gs} is increased because of the higher rate of impact-generation due to the increased in the electron current through the channel.

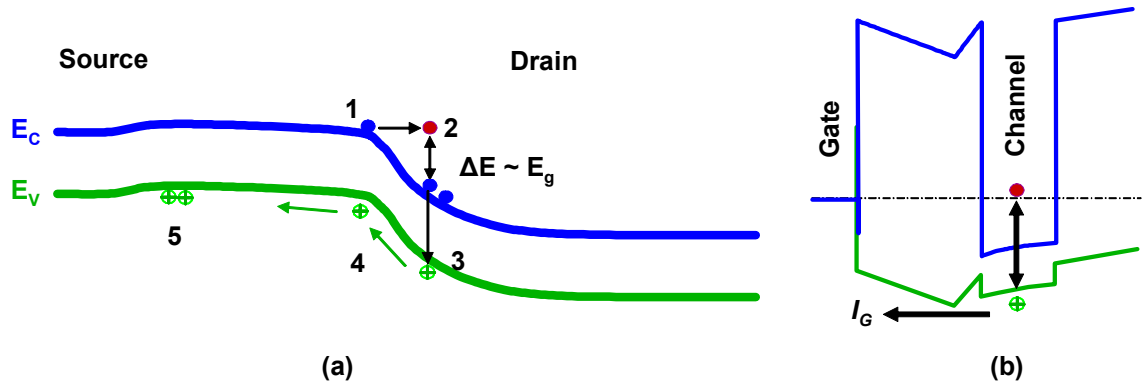


Figure 6.12 Energy band diagrams illustrating the effects of impact-generated holes on (a) the drain current and (b) the gate leakage current

In the case where impact-generated holes collect at the gate-source region, the additional positive charge gates the HEMT by lowering the effective potential barrier for electrons in the source, causing an increase in the drain current. This additional drain current is observed in the increased DC g_m seen at drain voltages of 0.3 V and above in Figure 6.11(a). It is this positive feedback from impact-generated holes that is responsible for the increase in drain current due to impact ionization; impact-generated electrons represent a small contribution to the overall additional drain current as demonstrated by Brar and Kroemer using a back-gated InAs/AlSb HEMT [70]. Because the hole transport time between the drain and source sides of the InAs channel is much larger than that of the electrons, the enhancement of the transconductance and output conductance are expected to have a strong frequency dependence at low microwave frequencies. The nature of this frequency dispersion is described experimentally and discussed in the following chapter.

CHAPTER 7

RF AND NOISE CHARACTERIZATION OF InAs/AlSb HEMTS

7.1. Introduction

A number of emerging systems applications such as active-array space-based radar, mobile millimeter-wave communications, and handheld imagers place a very high premium on speed-power performance. For such uses, InAs/AlSb HEMTs are especially promising because of their combination of high electron mobility, high peak velocity, and high electron concentration in the 2DEG that allows for ultra-low voltage operation The InAs/AlSb HEMT's inherent low voltage operation, with drain bias voltages below 0.5 V, can reduce DC power dissipation by an order of magnitude compared with a GaAs PHEMT of equivalent speed performance [72], [73], and by a factor of three to four compared to an equivalent InP HEMT [74], [75].

Besides the initial goal of developing the InAs/AlSb HEMT into a MMIC compatible technology, there was a need to improve the power gain of the transistor, as indicated by its low f_{max} figure of merit relative to other HEMT technologies. To date, the major inherent limitation of the InAs/AlSb HEMT has been the high output conductance associated with its low soft breakdown voltage due to the narrow bandgap of InAs (E_g = 0.36 eV). At microwave frequencies, the increased output conductance causes a proportionate reduction the maximum available gain from the device. The best reported figures of merit prior to this work indicate simultaneous f_τ / f_{max} of 250 / 80 GHz for a 0.10 μm gate length HEMT [76], and 160 / 110 GHz for a 0.15 μm HEMT [77]. The pad parasitic capacitances have been de-embedded from the measured s-parameters in the f_τ

calculation in both cases. Approaches to improve the breakdown characteristics in the InAs/AlSb HEMT include the use of a p-GaSb layer to collect impact-generated holes [70] and the use of an InAs sub-well composite channel design [5]. The p-GaSb back-gate approach was shown to be effective in lowering the DC output conductance through increased breakdown voltage, but the high frequency performance was degraded by the large shunt capacitance between the channel and back-gate. The sub-channel can improve breakdown slightly by shifting the electron transport to the narrow InAs sub-channel, but reported results show lowered electron mobility compared to single-channel InAs/AlSb HEMTs. In addition, the difficulty of engineering the device band structure and doping profiles so that the hot electrons are effectively transferred to the InAs sub-channel in the high field region complicates the HEMT epitaxial design.

Alternatively, we focus on ultra-low voltage operation, with drain bias voltages below 0.5 V, and do not modify the baseline InAs/AlSb HEMT shown in Figure 6.1 to increase the breakdown threshold. Section 7.2 describes the performance of such InAs/AlSb HEMTs with 0.2 μm gates with best-to-date simultaneous f_τ / f_{max} values of 170 / 195 GHz at drain bias voltages of only 0.3 V. Section 7.3 focuses on some of the remarkable effects of impact-ionization at RF frequencies, as introduced in the context of the HEMT DC characteristics in Section 6.5 of the previous chapter. Section 7.4 reports on the first comprehensive RF noise characterization of the InAs/AlSb HEMT. Finally, Section 7.5 briefly summarizes a demonstration of the first InAs/AlSb integrated circuit, a Ka-band low-power low-noise amplifier.

7.2. Small-Signal RF Performance

The epitaxial layer structure, fabrication process, and DC characteristics were described previously in Sections 6.1, 6.4, and 6.5 of Chapter 6, respectively. On-wafer s-parameter measurements were conducted from 0.05-50 GHz over a range of DC bias conditions. Contour maps of the -20 dB/decade extrapolated f_τ and f_{max} were generated, shown in Figure 7.1 for a $2 \times 20 \times 0.2$ μm HEMT, with f_τ and f_{max} mapped as a function of the DC drain bias condition. Pad parasitic capacitances were carefully measured on pad test structures and de-embedded from the RF short-circuit current gain h_{21} used in the calculation of f_τ.

We observe that f_τ increases monotonically with V_{ds} at drain voltages below approximately 0.25 V, in agreement with behavior the measured DC g_m shown in Figure 6.11(a). Above drain voltages of 0.3 V, however, f_τ slowly saturates with respect V_{ds} to a maximum of value of 180 GHz at $V_{ds} \geq 0.4$ V. This behavior can be understood by observing the dependence of the steady-state microwave g_m on the drain bias voltage, as shown in the RF g_m contour map in Figure 7.2. At drain bias voltages above about 0.3 V, the RF g_m saturates in a manner consistent with that of f_τ, leveling off to a maximum of 1.14 S/mm at $V_{ds} = 0.45$ V. This saturation is expected for a HEMT, and merely confirms that the large peak DC g_m observed in Figure 6.11(a) at drain voltages above 0.25 V is an artifact of the kink effect. In contrast, there is a well-defined peak in f_{max}, reaching a maximum of 195 GHz occurring at a drain voltage of 0.3 V. The decrease in f_{max} with respect to further increases in V_{ds} above 0.3 V is a consequence of higher output conductance caused by the onset impact ionization.

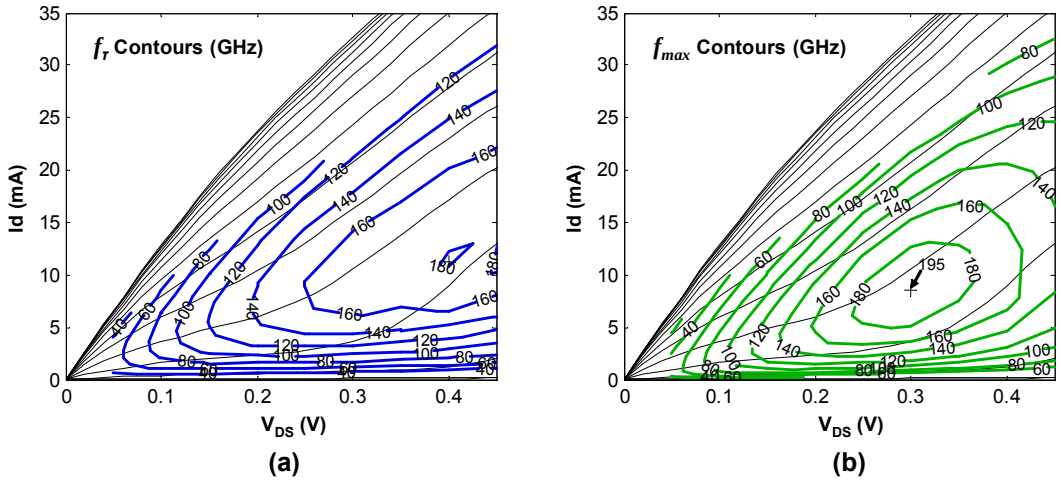


Figure 7.1 (a) The f_τ contour plot for a $2 \times 20 \times 0.2$ µm HEMT. (b) The corresponding $f_{\max}$ contour plot.

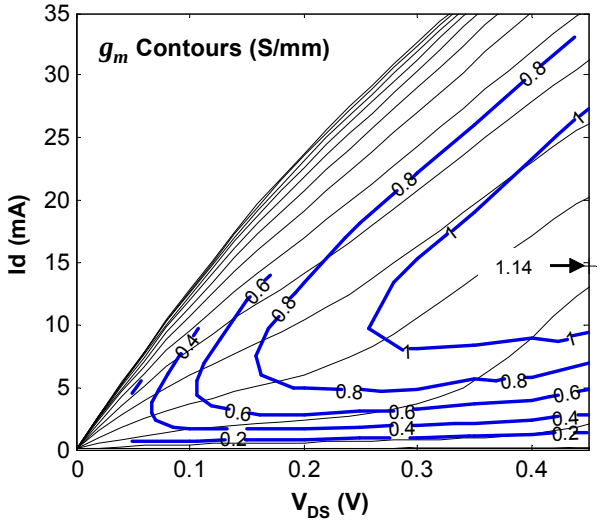


Figure 7.2 Contour plot of the measured extrinsic RF g_m.

The peak simultaneous f_τ / $f_{\max}$ values are 170 / 195 GHz, occurring at a drain voltage of only 0.3 V. Figure 7.3 shows the extrapolation of f_τ and $f_{\max}$ from h_{21} and the unilateral gain U at this bias point. The f_τ-L_g product of 36 GHz-µm is excellent for any 0.2 µm HEMT technology, while the peak $f_{\max}$ value of 195 GHz exceeds the best prior

published value by 75% [77]. The potential for extreme low voltage operation is demonstrated by the attainment of f_τ and f_{max} peak values of 90 and 95 GHz, respectively, at a degraded drain bias of only 0.1 V. Such ultra-low voltage operation is made possible by the very low drain saturation voltages due to the high electron mobility in the InAs channel.

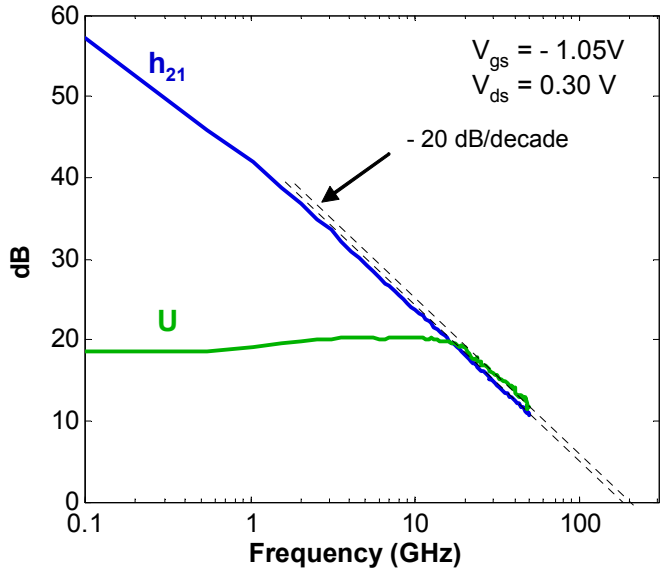


Figure 7.3 The 2 × 20 ×0.2 μm HEMT's short-circuit current gain, h_{21}, and maximum unilateral gain, U.

Figure 7.4 shows a compilation of published HEMT results to date. The 0.25 μm and 0.5 μm gate length results published by our group were based on a prototype HEMT wafer with both a thicker barrier (250 Å vs. 180 Å) and an increased 2DEG electron concentration (5×10^{12} cm^{-2} vs. 3.7×10^{12} cm^{-2}) [78]. As expected, f_τ scales inversely with the gate length, but f_{max} does not show significant dependence on L_g. We believe that the superior f_{max} obtained in this work over those published previously is generally

attributable to the increased charge in the 2DEG in this HEMT made possible by doping with PbTe. Note that the vertical scaling of the HEMT published in [79] relative to the HEMT reported in [78] nearly doubled f_{max}, although the comparison is of limited value because the HEMT in [78] also showed a higher output conductance. Nevertheless, further vertical scaling of the top barrier is expected to improve the transistor's speed, through a proportionally increased transconductance.

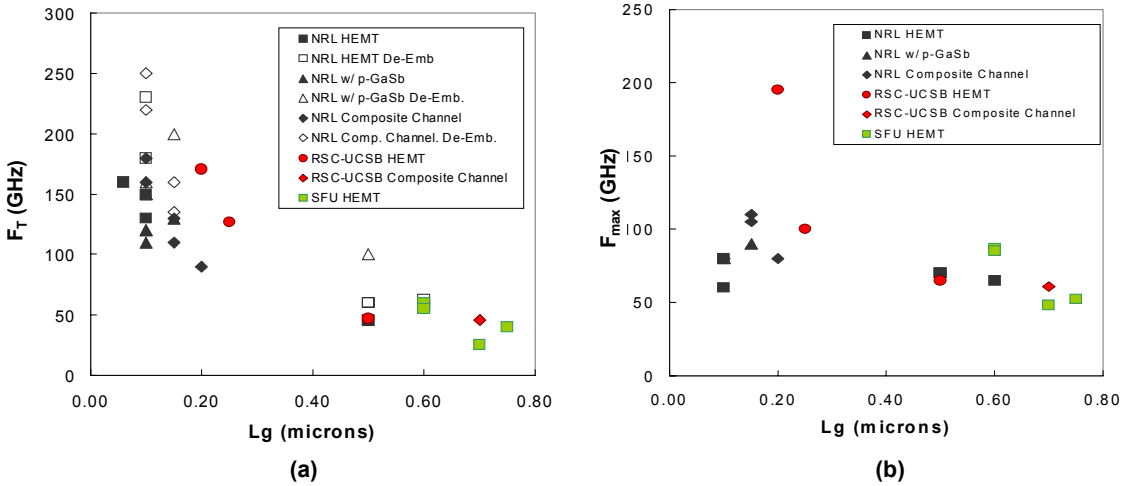


Figure 7.4 (a) Compilation of f_τ for various published InAs/AlSb HEMTs. (b) The corresponding published f_{max} values.

7.3. Effects of Impact Ionization at RF Frequencies

Recall from Chapter 6 and earlier in this chapter in Section 7.2 that impact ionization of hot electrons in the high field region near the drain has an especially strong influence on the InAs/AlSb HEMT's electrical characteristics due to the narrow 0.36 eV bandgap of InAs. The products of the impact ionization on the HEMT DC characteristics discussed in Chapter 6 can be divided into three main external effects. First, soft

breakdown at high drain biases increases the output conductance as was clearly visible in the HEMT output characteristics in Figure 6.10. Second, the DC peak transconductance likewise was seen to increase dramatically at drain bias voltages above about 0.25 V due to the kink effect as was shown in Figure 6.11(a). Finally, the on-state gate leakage current (GLC) was also seen to increase exponentially with increasing drain voltage. All of these artifacts are attributable to impact-generated holes, as was proven experimentally by studying a four-terminal back-gated InAs/AlSb HEMT with a p-GaSb back-gate that could collect the impact-generated holes [70]. In this section and the one following, we see that all of these effects of impact ionization extend into microwave frequencies and impact the small-signal gain and noise characteristics in the RF regime.

The effect of impact ionization in the microwave regime at high drain bias is most clearly visible on the output impedance. At high drain bias, the output impedance is inductive, as seen in Figure 7.5, with the effect becoming far more pronounced as the drain bias voltage increases from 0.2 V to 0.4 V. To quantify this effect, consider the frequency at which the s_{22} crosses from the inductive regime to the capacitive regime. This crossover frequency increases rapidly with V_{ds}, going from 0.7 GHz at $V_{ds} = 0.2$ V, to 3.1 GHz at $V_{ds} = 0.3$ V, and reaching 9.7 GHz at $V_{ds} = 0.4$ V for a fixed gate bias. While this inductive output impedance at high drain bias has been observed in both lattice-matched [80] and psuedomorphic InGaAs HEMTs [81] on InP, the characteristic is much more pronounced in the InAs/AlSb HEMT due to its narrower bandgap. While the microwave impedance is referred to as inductive, it should be noted that this term only applies in the sense of the relative phase of the current to the voltage at the output, not in the physical sense of energy storage in a magnetic field. The reason that s_{22}

appears inductive at low frequencies is the relatively slow diffusion time between the generation of excess holes by impact ionization and their accumulation at the source side of the channel where they can lower the barrier to inject more electrons. This time delay in the positive feedback mechanism between the drain voltage and the drain current due to the kink effect causes the AC drain current to lag the voltage at low frequencies.

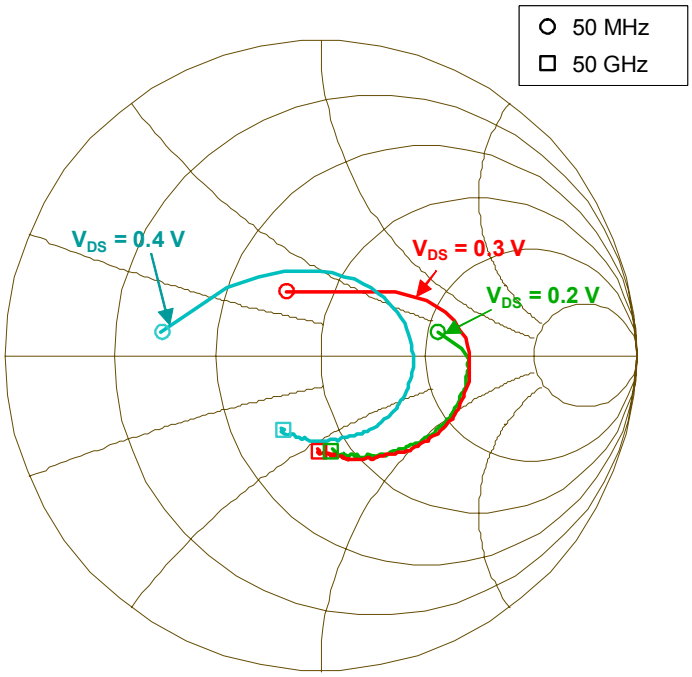


Figure 7.5 The measured s_{22} from 0.05-50 GHz for V_{ds} = 0.2, 0.3, and 0.4 V, at a gate voltage of -1.05 V.

The second major effect of impact ionization is the enhancement of the InAs/AlSb HEMT's transconductance evident at high drain bias and low frequencies. Recall that the DC peak transconductance continued to increase with drain bias, increasing approximately in proportion to the drain voltage as V_{ds} was stepped from 0.1 to 0.4 V, reaching peak values over 2.0 S/mm. This behavior opposes the conventional HEMT's

saturation of g_m with drain voltage. Because the high g_m values are related to gating by impact-generated holes, the anomalously high transconductance observed for $V_{ds} \geq 0.3$ V, is not expected to be part of the steady-state microwave g_m. This expectation is met when the AC steady-state g_m is compared against the DC g_m, as is done in Figure 7.6. The intrinsic steady state g_{mi}, given by

$$g_{mi} = \frac{g_{me}}{1 - R_s g_{me}} \tag{7.1}$$

is both lower and much less sharply peaked than its DC counterpart. (The steady-state RF extrinsic transconductance g_{me} is simply the real part of y_{21} and R_s is the source access resistance. R_s is computed from the measured DC drain-to-source resistance R_{ds} at zero gate and drain bias scaled by the nominal source-to-gate spacing. For the $2 \times 20 \times 0.2$ μm HEMT reported here, R_s is 3 Ω.) The improved linearity of the RF g_m with respect to V_{gs} and I_d relative to that of the DC g_m is beneficial in amplifier applications where the HEMT linearity dictates the amplifier dynamic range. Note also that unlike the DC g_m, the RF g_m saturates with respect to V_{ds}, in agreement with the behavior of conventional GaAs and InP HEMTs.

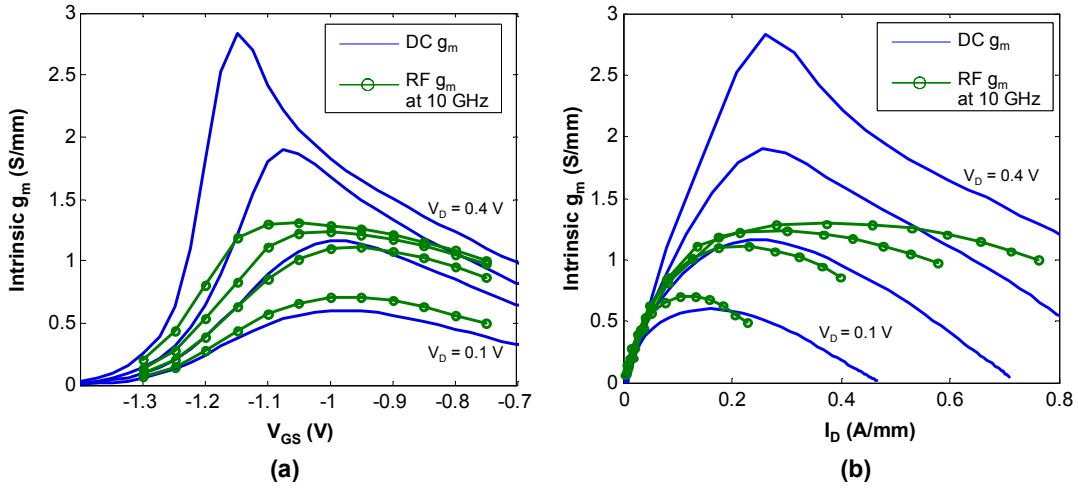


Figure 7.6 The steady-state microwave transconductance plotted with the DC transconductance as a function of (a) V_{gs} and (b) I_d.

The small-signal equivalent circuit schematic shown in Figure 7.7 helps identify the various components of the common-source transistor two-port network. It is a conventional hybrid-π HFET model that adds an additional current source denoted by y_{ii} to the output to include the kink effect at microwave frequencies. The parasitic capacitance of the probe pads at the source and drain are modeled by C_p, a simple lumped capacitor. The inductive components do not represent a significant contribution to the source and drain pad parasitics below millimeter-wave frequencies, and are not included here.

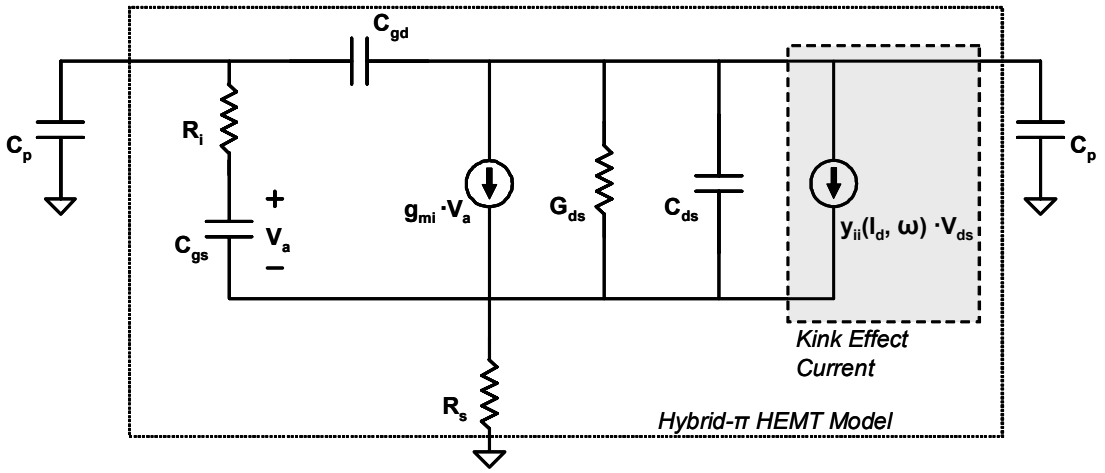


Figure 7.7 Small-signal hybrid-π equivalent circuit for an InAs/AlSb HEMT, with additional current source to model the effects of impact ionization on the drain current.

The current source y_{ii} relating to the kink effect caused by gating of impact generated holes is difficult to model as a lumped linear current source, because it is simultaneously dependent on both the drain current modulation and the drain voltage modulation. The rate of hole generation is a function of the drain voltage because the probability of impact ionization per electron is exponentially dependent on V_{ds}. The rate also depends linearly on the drain current because I_d determines the number of hot electrons that are available for impact ionization. Furthermore, y_{ii} is also frequency dependent, reflecting the time delay in the feedback path between the impact-generation of holes at the drain and the gating effect at the source. A simple model for y_{ii} that consists of a series connect resistor and inductor [82] is of limited value because it is generally ill-conditioned with respect to the DC bias condition, and does not reflect the enhancement of the low-frequency transconductance by the kink effect.

While a good analytical representation for the small-signal kink effect current source remains a subject for future investigation, significant understanding can be gained

by observing the frequency dependence of the forward transconductance and output conductance at different drain bias conditions. Figure 7.8(a) shows that the enhancement of g_m is limited to low frequencies. At V_{ds} = 0.1 V, there is no observable frequency dispersion, while at 0.2 V, the frequency dependence is slight: at 50 MHz the g_m is only 9% above its steady-state value, and it settles to within 2% of the steady state value at 0.5 GHz. At V_{ds} = 0.3 V, there is a 45% enhancement in g_m at 50 MHz, settling to within 2% of the steady state value at a frequency of 1.8 GHz. At V_{ds} = 0.4 V, the magnitude of the g_m enhancement and its decay frequency both increase, to 100% and 4.1 GHz, respectively. The increased drain current due to the kink effect augments the output conductance similarly, giving it a similar magnitude and frequency dependence. The relative contribution of the kink effect current is greater on the total output conductance than on the total transconductance because the static (not related to the kink effect) component of the g_{ds} is considerably smaller than the static component of the overall g_m.

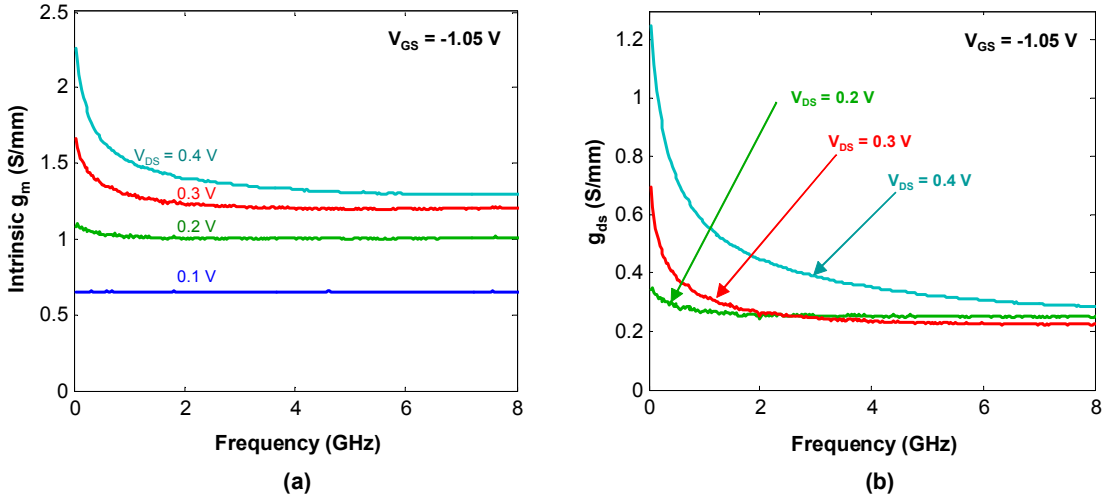


Figure 7.8 (a) The frequency dependence of the intrinsic transconductance. (b) The frequency dispersion of the output conductance.

7.4. RF Noise Characteristics

7.4.1. Introduction

There is only one previous published measurement of the RF noise figure of an InAs/AlSb HEMT, which gave brief mention to the RF noise characteristics of a 0.1 μm HEMT by Boos, *et al* [83]. Boos reported a minimum noise figure F_{min} in excess of 1 dB at all frequencies above 2 GHz for a 0.1-μm gate-length HEMT, with the measured F_{min} slightly exceeding 2.0 dB at 18 GHz, the highest frequency measured. No bias dependence was presented, and the effect of gate leakage was briefly mentioned as contributing to the noise. In this section, the results of a comprehensive RF noise parameter characterization of the InAs/AlSb HEMT are presented, showing superior minimum noise figure ($F_{min} \leq 1.0$ dB) up to 25 GHz, along with an analysis of the dependence of the noise figure on the DC bias state of the HEMT. The identification of the various intrinsic noise sources, and their corresponding bias and frequency dependence gives significant insight toward the optimization of the InAs/AlSb HEMT for high-frequency low-noise amplifiers (LNAs).

We start by identifying the expected sources of noise in the intrinsic InAs/AlSb HEMT. Figure 7.9 illustrates the various noise mechanisms in the HEMT from a perspective of the electron transport. These noise sources are divided into three general categories: thermal noise, shot noise, and impact-generation noise, which differ in their respective noise spectra. Thermal noise is associated with the intrinsic FET series resistances in the gate and source. Its noise power density given by $4kTR$, in which T is the ambient temperature, and R is the resistance. Diffusion noise has a similar form

expressed by a noise current $\langle i^2 \rangle = 4kTg_m\Gamma \cdot \Delta f$ at the output, where Γ is a correlation factor. The diffusion noise will be grouped with the thermal noise from this point onward. Note that the thermal noise is white noise, i.e., it is frequency independent. Shot noise is represented by a noise current $\langle i^2 \rangle = 2qI \cdot \Delta f$, where I is the mean current. Finally, the generation of carriers by impact ionization adds additional noise. If the impact ionization rate can be characterized by a time constant τ_i, then the spectral density of the impact-generation noise has a Lorentzian frequency dependence [80], [81], so that

$$S(f) \propto \frac{\tau_i}{1+\omega^2\tau_i^2}, \tag{7.2}$$

where $\omega = 2\pi f$.

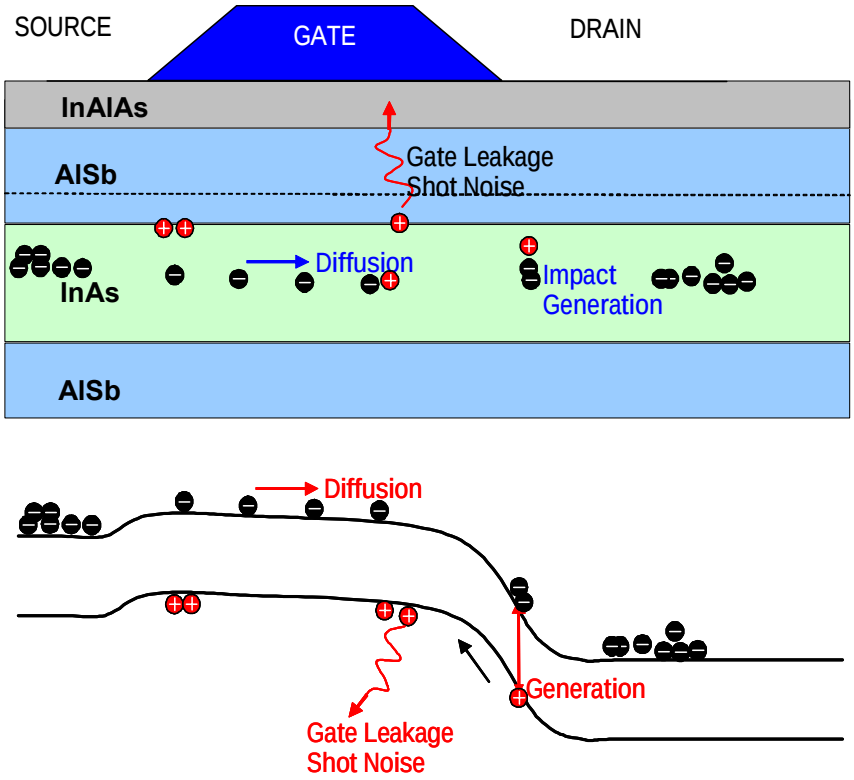


Figure 7.9 The various noise mechanisms present in an InAs/AlSb HEMT

Because the diffusion noise adds to the output noise, it causes the FET noise figure to increase approximately linearly with frequency. Although the output noise source is frequency independent, the input signal gain rolls off inversely with frequency, causing the signal-to-noise ratio at the output to increase monotonically with frequency, as is captured in the classic Fukui equation for the microwave FET noise [84],

$$F_{\min} = 1 + 2k_f \frac{f}{f_\tau} \sqrt{g_m (R_s + R_g)}\,, \tag{7.3}$$

where k_f is a technology dependent parameter. Please note that there is a g_m factor in the denominator of the second term, since $2\pi f_\tau = g_m / (C_{gs} + C_{gd})$, and the higher g_m would result in a lower noise figure. While a Fukui-like frequency dependence is characteristic when thermal noise is the dominant noise source, additional noise sources can alter the

noise figure and its frequency dependence. The GLC, in particular, adds a shot noise component at the amplifier input which adds a uniform excess noise to the overall noise figure at all frequencies [85]-[87]. Finally, the impact-generation noise, if present, adds a Lorentzian noise source at the output which adds a $1/f$ noise to the total FET noise figure. These three basic noise mechanisms and the frequency dependence that they impart to the noise figure are summarized in Table 7.1.

Table 7.1 RF noise sources in InAs/AlSb HEMTs and their frequency dependence in the noise figure.

	Source of Noise	Frequency Dependence
Thermal Noise	Carrier Diffusion, Resistances	f/f_τ
Input Shot Noise	Schottky diode Leakage	Constant
	Impact-generated hole gate current	
Impact-Generation	Impact-ionization	$1/f$

7.4.2. Results and discussion

The noise parameters of a $2 \times 20 \times 0.3$ μm InAs/AlSb with peak f_τ and f_{max} of 130 and 180 GHz (refer to Chapter 6 for the epitaxial layer structure and fabrication process) were measured on-wafer using a Hewlett-Packard 8570B/8571C noise figure meter and test set and an HP 346C solid-state noise source. An ATN solid-state tuner was used to vary the source impedance presented to the HEMT, and an HP 8510C network analyzer measured the impedance and gain.

Figure 7.10 shows three different HEMT DC operating points, each illustrating one or two of the three basic noise mechanisms described in Section 7.4.1. At V_{ds} = 0.1 V (Figure 7.10(b)) the thermal noise is the dominant noise source, as can be deduced from the monotonic increase in F_{min} with respect to frequency. This observation is consistent with the low GLC of 1.0 μA at this bias. At 2 GHz, the lowest frequency measured, the minimum noise figure was 0.4 dB. F_{min} rises quickly as the frequency increases, which is expected because the HEMT f_τ is only 58 GHz at this operating point. At V_{ds} = 0.2 V (Figure 7.10(c)), we observe that the rate of increase of F_{min} with frequency is lower on account of the higher f_τ of 97 GHz. The result is a minimum noise figure of 1.0 dB at 25 GHz, which represents record RF noise performance for a HEMT in this material system. There is an excess noise at all frequencies due to the gate leakage current of 3.4 μA. The noise figure at V_{ds} = 0.4 V (Figure 7.10(d)), however, is significantly higher at all frequencies compared to that measured at lower drain voltages. The cause of the high F_{min} of approximately 2.5 dB from 10-25 GHz is the input shot noise resulting from the high GLC of 38 μA. Most of this gate leakage is the hole current arising from the collection of impact-generated holes by the gate. Finally, note that the minimum noise figure at V_{ds} = 0.4 V decreases with increasing frequency below 10 GHz, indicating that impact-ionization is limiting the noise figure in this regime. The frequency dependence of F_{min} is in this case primarily an effect of the G_{ds} dispersion (caused by impact-generated holes) rather than of the Lorentzian spectral density of an impact-generation noise.

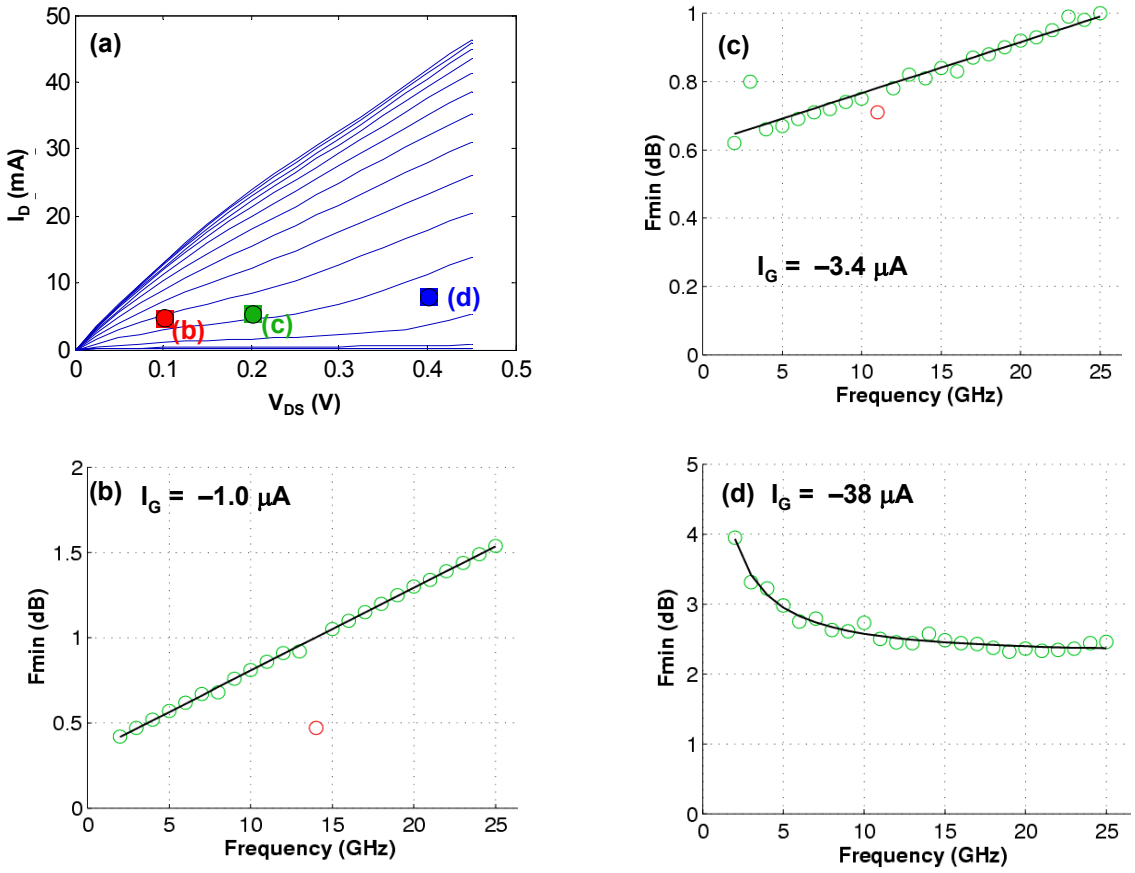


Figure 7.10 (a) The DC operating point for the three plots minimum noise figure plots at (b) V_{ds} = 0.1 V, (c) V_{ds} = 0.2 V, and (d) V_{ds} = 0.4 V.

The F_{min} contour plots of Figure 7.11 allow the optimum bias for the lowest possible noise figure to be determined at a given frequency of operation. As can be seen in Figure 7.11(a), the optimum bias for low noise at 2 GHz occurs at drain bias voltage close to 0.1 V. This result is unexpected if the HEMT noise sources were assumed to be primarily thermal in nature. Since $(F_{min}-1)$ is proportional to f/f_τ when the HEMT noise arises from thermal noise sources and the frequency is well below f_τ, the optimum drain bias would be expected to be at a higher drain voltage, where f_τ is higher. At the optimum bias point for minimum noise, the measured f_τ is only 58 GHz. From the F_{min} bias dependence observed in Figure 7.11(a), it is reasonable to suspect that the excess noise arising from the input shot noise from gate leakage dominates the overall HEMT noise figure at 2 GHz, since the GLC increases with increasing drain bias. At the optimum bias point, the gate current is low, approximately 1 μA.

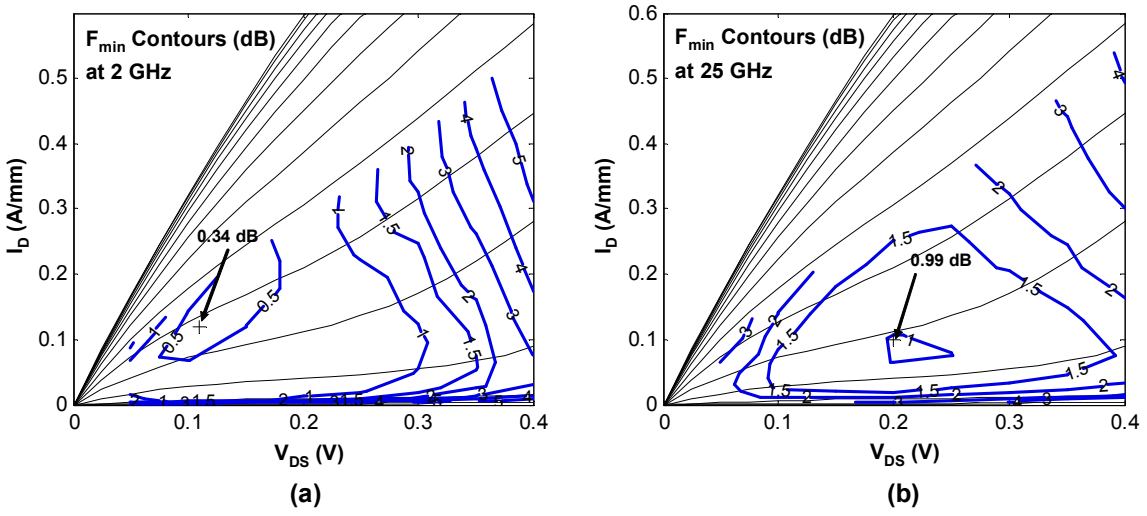


Figure 7.11 (a) The contour plot of F_{min} at 2 GHz as a function of the drain bias. (b) The F_{min} contour plot at 25 GHz.

In contrast, the F_{min} contour maps of Figure 7.11(b) show that the optimum bias for the lowest noise at 25 GHz shifts from 0.1 V to 0.2 V, because the increased contribution from thermal noise favors higher drain voltages where f_τ is higher. At the 25 GHz optimum bias point, F_{min} is 1.0 dB, f_τ is 97 GHz, and the GLC is 3.4 μA. It is worth noting that at all frequencies measured the optimum drain current bias occurs at approximately 0.1 A/mm, which is consistent with the behavior of GaAs PHEMTs and InP-based HEMTs. Finally, observe that the minimum noise figure at 2 GHz increases very rapidly with drain voltage for $V_{ds} \geq 0.3$ V. This effect is a consequence of the increased RF output conductance at low frequencies in the InAs/AlSb HEMT at this voltage.

To fully appreciate the dominance of the GLC induced shot noise on the overall noise figure, the GLC and minimum noise figure are plotted together in the parametric F_{min} color map shown in Figure 7.12. At 2 GHz, F_{min} tracks the GLC nearly perfectly, showing that the gate leakage shot noise is the dominant noise source in the low gigahertz frequency range. At 25 GHz, we note that there is less correlation between F_{min} and the GLC because thermal noise comes into play, although at drain bias voltages above approximately 0.25 V, the GLC is high enough that the input shot noise dominates the thermal noise in the overall HEMT noise figure.

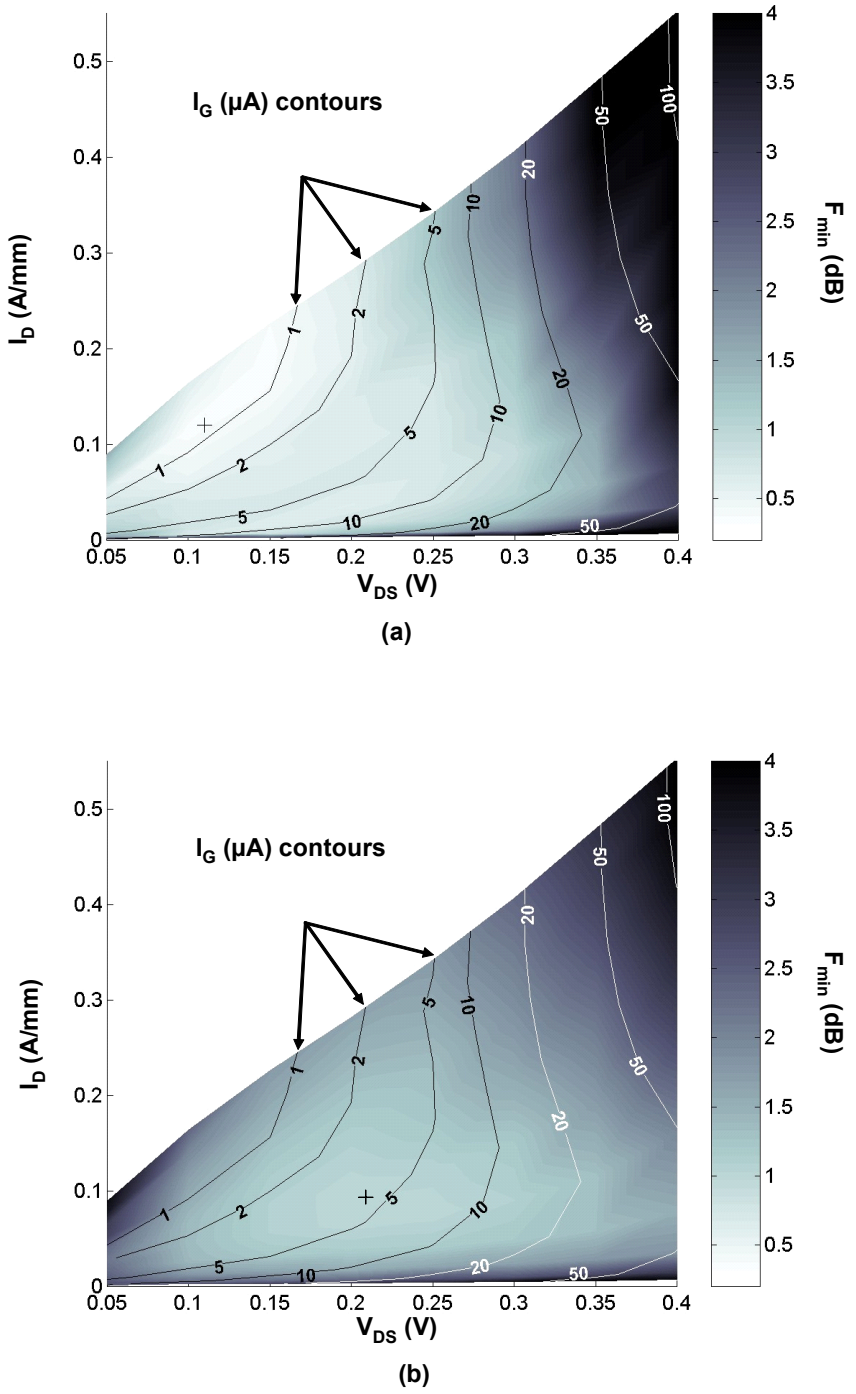


Figure 7.12 (a) Parametric color map of the minimum noise figure at 2 GHz overlaid by the gate leakage contours. (b) The corresponding map of F_{min} and I_g at 25 GHz.

The drift of the optimum bias point toward higher bias points as the frequency increases is beneficial because the HEMT offers improved gain as the drain bias increases. Figure 7.13 plots the associated gain at 25 GHz as a function of the drain voltage and current. At a drain voltage of 0.1 V, the associated gain (G_{assoc}) is no more than 6 dB. At $V_{ds} = 0.2$ V, the optimum bias for the lowest noise at 25 GHz, G_{assoc} increases to 11 dB. Still, this is somewhat lower than the peak gain of 13.6 dB at a drain voltage of 0.35 V, indicating the fundamental tradeoff between noise figure and gain. Nevertheless, the overall trend of increasing drain voltages to achieve the optimum noise figure is encouraging as the InAs/AlSb HEMT is considered for Ka-band and millimeter-wave low-noise amplifiers.

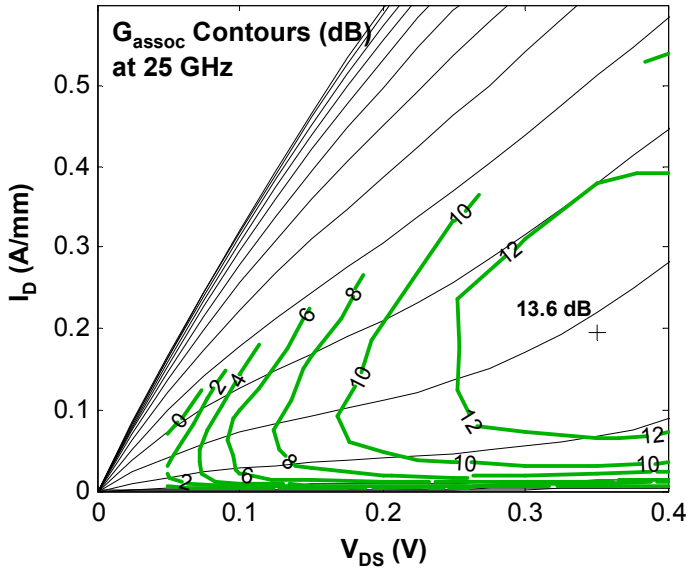


Figure 7.13 The associated gain contours at 25 GHz.

7.4.3. Looking ahead to higher frequencies

Because the bandwidth of the noise figure tuners and noise figure meter is limited to 26 GHz, the noise parameters cannot be measured at higher frequencies. Nevertheless, simple simulations were performed that will allow the behavior of the noise figure at higher frequencies to be anticipated. The simplified noise equivalent circuit of Figure 7.14 was simulated in Agilent's Advanced Design System (ADS) Microwave CAD software. The gate leakage shot noise was modeled by a noise current generator at the input I_{gn} with $\left\langle i_{gn}^2 \right\rangle = 2qI_g\Delta f$, where the GLC was a simulation input parameter. The diffusion noise is modeled by a noise current source I_{dn} at the output with $\left\langle i_{dn}^2 \right\rangle = 4kTg_m\Gamma\Delta f$.

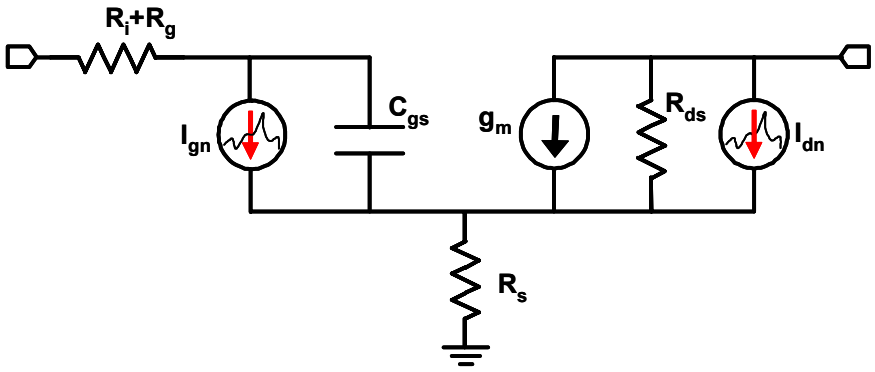


Figure 7.14 The noise equivalent circuit used for simulating the HEMT noise figure above 25 GHz.

Figure 7.15(a) shows the effect of increasing the HEMT f_τ on the minimum noise figure as a function of frequency in the ideal case of zero gate leakage. The effect of increasing f_τ was modeled by scaling C_{gs} in inverse proportion to the specified f_τ, which approximates a reduction of the gate length in an actual HEMT. The predicted minimum

noise figure exhibits Fukui-like behavior, with (F_{min}−1) increasing in proportion to f/f_τ. For a given HEMT f_τ, the addition of a GLC is observed to degrade F_{min} at low frequencies, in agreement with the experimental observations in Section 7.4. As seen in Figure 7.15(b) the GLC adds an excess noise at low frequencies but becomes less of a factor in the overall noise figure at higher frequencies where the monotonically increasing thermal noise is dominant. The approximate frequency f_{sh} at which the contribution of thermal noise to the overall noise figure overtakes that of the gate leakage induced shot noise is given by [86]

$$f_{sh} = f_\tau \sqrt{\frac{qI_g}{2g_m \Gamma kT}}. \tag{7.4}$$

This relation signifies that the relative impact of the GLC on the overall total figure increases not only with the GLC but also with the transconductance g_m. Due to the high transconductance inherent in InAs/AlSb HEMTs, the GLC should have a more significant effect on the HEMT noise figure than conventional GaAs and InP-based HEMTs.

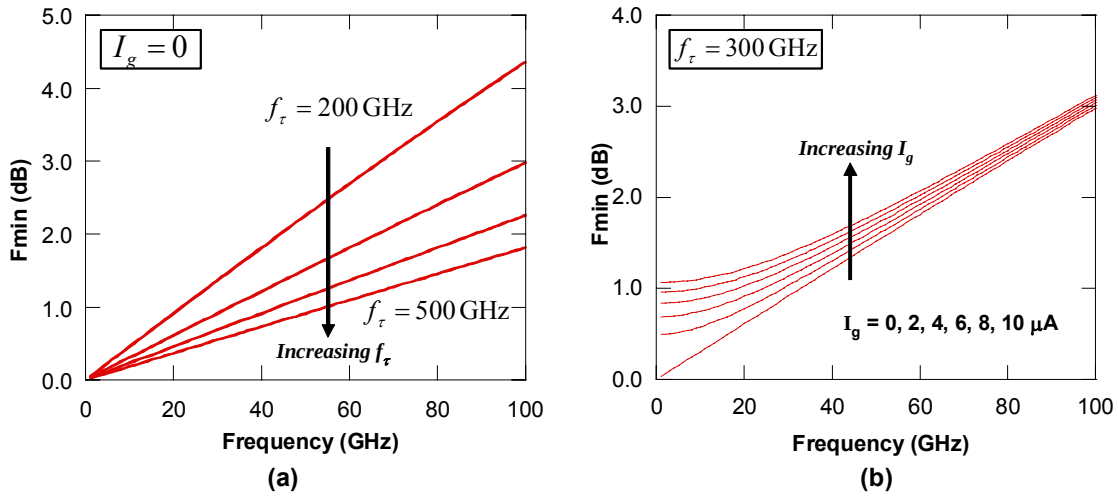


Figure 7.15 (a) Simulated minimum noise figure for the equivalent HEMT model of Figure 7.14 with varying f_τ and zero gate leakage. (b) Simulated minimum noise figure for a HEMT with f_τ = 300 GHz with gate leakage included.

The conclusion to be drawn from the simulation results up to 100 GHz and the experimental HEMT noise figure data up to 25 GHz is that the effect of the GLC on the overall noise figure dictates both the optimal HEMT epitaxial design and the optimal bias condition for the HEMT. For low-noise applications below about 10 GHz, the HEMT epitaxial design can be modified to sacrifice speed (f_τ) for reduced gate leakage, as could be achieved by employing thicker barriers. Also, the drain bias voltage can be reduced to minimize the gate leakage at the expense of gain, which can be accomplished more readily at low frequencies where the HEMT gain is higher. On the other hand, at high frequencies such as in W-band applications near 100 GHz, the HEMT must offer sufficient gain to be useful as an LNA stage. In this case, the drain bias voltage can be increased to increase the stage gain because the contribution of shot noise from gate leakage to the noise figure is much smaller relative to that of the thermal noise sources at this frequency. Additional vertical scaling of the HEMT barriers will also improve the

speed of the transistor, with the price of higher gate leakage likewise being justified due to its lesser impact at higher frequencies.

7.5. InAs/AlSb MMIC Demonstration: A Ka-Band Low-Power Low-Noise Amplifier

The first antimonide-based MMIC, a three-stage Ka-band low-power low-noise amplifier (LP-LNA) using the 0.25 μm InAs/AlSb metamorphic HEMT, was fabricated and characterized on a GaAs substrate [88]. The MMIC design and layout was performed by J. Hacker, who designed the LNA based on measured s-parameters from a prototype InAs/AlSb HEMT. The design was conducted without the benefit of the noise characterization presented in this work. The LNA was fabricated using the baseline InAs/AlSb MMIC process described in Chapter 6. The final first-pass three-stage LNA is pictured in Figure 7.16.

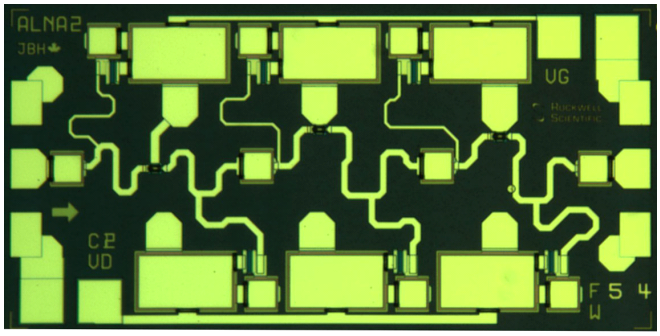


Figure 7.16 Photomicrograph of the three-stage InAs/AlSb HEMT Ka-Band LNA MMIC. The compact die measures 1.5 mm × 0.7 mm.

The performance of the LP-LNA was measured on-wafer using RF probes. The measured amplifier noise figure averages 2.1 dB over the 34-36 GHz frequency band specified in the design, with a corresponding average gain of 21.8 dB. The gain and noise figure measurements are shown in Figure 7.17. The most impressive aspect of the LP-LNA is the very low DC power consumption made possible by the low drain saturation voltage of the InAs/AlSb HEMT. The LP-LNA operated with a supply voltage and current of 0.35 V and 12.8 mA, respectively, corresponding to a DC power consumption of 4.5 mW. This DC power consumption is less than one-tenth that of an GaAs PHEMT-based LNA that requires a 2.0 V drain bias voltage, and one-third that of an InP-based LNA that requires 0.75 V drain bias. The speed and noise performance of the InAs/AlSb HEMT MMIC technology promises to improve as gate lengths are scaled, the epitaxial layer structure is refined, and device characterization experience is incorporated into the circuit design process.

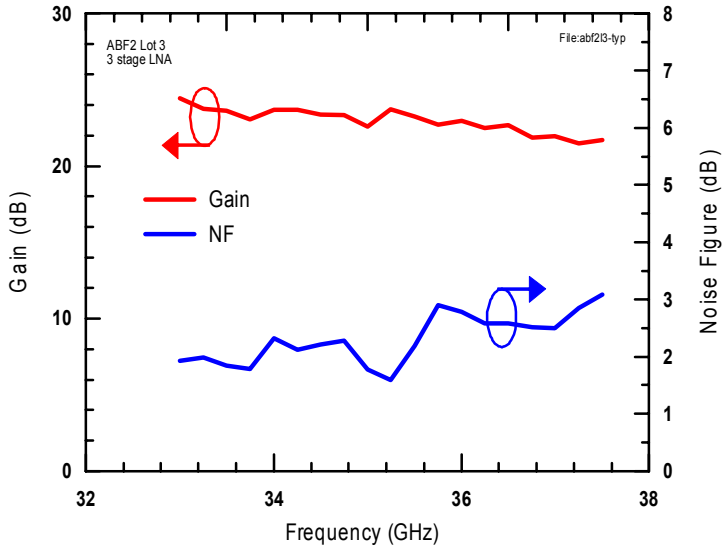


Figure 7.17 Measured noise figure and associated gain of the InAs/AlSb three-stage LP-LNA.

CHAPTER 8

CONCLUSIONS AND FUTURE WORK

8.1. Technical Contributions

This dissertation has presented different approaches to the realization of integrated InAs-based electron devices in microelectronic circuits, focusing on the InAs-well RTD and the InAs/AlSb HEMT as the active devices to be integrated in circuits. Two different approaches were followed, the hybrid integration and the monolithic integration methods. The desirability of a hybrid integration approach for improved performance, as in the case of back-gated InAs-based HEMTs, and its necessity, as in the case of integrated silicon-RTD electronics, have been outlined. Monolithic integration has likewise been discussed in terms of the tunnel diode-based QMMIC technology and the metamorphic InAs/AlSb HEMT MMIC technology. In general, monolithic integration, where possible, has the advantage of ease of implementation, while hybrid integration offers maximum flexibility for device and circuit optimization to push performance to its ultimate limits.

8.1.1. Successful RTD-CMOS hybridization

This work includes the first report of a single-chip RTD-CMOS circuit that was demonstrated using the planarized thin-film integration method outlined in Chapter 3, with the clocked quantizer serving as a demonstration. This planarized thin-film integration technique differs from those of previous reports in that allows devices that do

not have a strictly planar geometry to be integrated in the same fashion as the planar devices.

8.1.2. Reduction of the parasitic elements in thin-film RTDs

The next step in the development of the thin-film hybrid integration of RTD-CMOS circuits was to optimize the processed RTD structure on the InP substrate before substrate removal in order to minimize the parasitic capacitance which was over 1 pF, an impractically large number. An analysis of the components of the parasitic capacitances associated with the thin-film integration process identified the limiting factors in dictating the switching speed of a thin-film integrated RTD-CMOS circuit, and identified the tradeoffs inherent in the fabrication process. This analysis suggested that the total parasitic capacitance could be scaled to the order of the RTD intrinsic capacitance for RTD areas of $1.4 \times 1.4\ \mu m^2$ and larger. The capacitance distribution and corresponding analysis is equivalent for any hybrid of high-speed electronic devices onto silicon host substrates that use the same thin-film integration method. The thin-film RTD structures fabricated in the process developed using this analysis showed on-wafer yields greater than 95%.

8.1.3. Development of a MMIC compatible InAs/AlSb HEMT

The latter part of this dissertation focused on the development of a MMIC-compatible InAs/AlSb HEMT. The initial obstacles that were addressed and successfully resolved dealt with fundamental material problems, namely the micro-crack formation during MBE growth and buffer oxidation problems. The actual HEMT fabrication needed significant refinement in order to obtain reproducible ohmic contacts with

resistances below 0.07 Ω-mm with Pd-based ohmic contacts that are needed for a viable low-power, low-noise, and high-frequency MMIC technology. The RF performance of the InAs/AlSb HEMT yielded best-to-date speed in the 6.1 Å material system, with simultaneous measured f_τ / f_{max} values of 160 / 190 GHz for a 0.2 μm gate length HEMT. The RF noise characterization of a 0.3 μm InAs/AlSb HEMT was the first such measurement to show the complete bias dependence of the RF noise at frequencies up to 25 GHz in this technology, and has improve both device design and circuit design for InAs/AlSb HEMT-based low-noise amplifiers. Finally, the RF measurements performed in this work and the MMIC fabrication process developed in tandem enabled the design and fabrication of the first ever antimonide-based MMIC, a three-stage Ka-band LNA with ultra-low power dissipation.

8.2. Impact of the Work in Real Applications

8.2.1. InAs/AlSb HEMTs on GaAs substrates

The InAs/AlSb HEMT work done in this dissertation demonstrates that the most obvious and easily achieved advantage of this technology is the potential for high-speed operation with ultra-low power dissipation. The bias dependence of both the RF power gain and the RF noise figure (at 25 GHz) shows that the performance peaks occur at drain voltages of only 0.3 V and 0.25 V, respectively. These low voltages translate directly into very low power consumption, with static power dissipation reduced by nearly a factor of 10 relative to GaAs-based MMICs, and a factor of 3 relative to InP-based MMICs. The ultra-low power dissipation of the InAs/AlSb HEMT makes it an enabling technology for RF applications in which a high premium is placed on the receiver power

consumption. Such potential applications include X-band satellite-based communications in which arrays of tens of thousands of receivers must be listening continuously, and in novel circuits that are powered by unconventional sources that supply very limited power.

8.2.2. Thin-film InAs quantum well RTD-CMOS hybrids

The thin-film hybridization approach to realize InAs quantum well RTD-CMOS circuits was always intended at best to be an early prototyping method, not a mature manufacturing process. Even with the improvements in the process developed in this work, the difficulty of the transfer and bonding process for a thin-film of RTDs that has multiple bond pads represents a major barrier to its implementation. Given these obstacles along with the rapid and implacable advance of silicon electronics, there will not likely be a future for hybrid circuits integrating CMOS and InAs quantum well RTDs, or any InAs-based electronic device. Nevertheless, chip-level substrate removal and transfer of InAs-based optoelectronics has much brighter future outlook. InAs/(In)GaSb strained-layer superlattice PIN photodiodes [89], [90] that are being developed for very-long wave infrared (VLWIR) imaging will require complete removal of the GaSb substrate to eliminate free carrier absorption in the substrate.

8.3. Future Research Directions

8.3.1. Improving the hybridization of the RTD

The thin-film transfer hybridization method used in this work has a few problems that make it difficult to implement successfully. The first difficulty is the delicacy of the

thin-film once the InP substrate has been removed. It would be preferable to keep the InP substrate in place to improve the mechanical integrity of the die to be bonded to the silicon chip, and this is feasible when there is no need to make a back contact to the RTD chip. In the next-generation thin-film RTD process detailed in Chapter 4, all discrete RTDs and multiple-RTD structures were available with front-side only bond pads in a planar array, and only the need for optical alignment necessitated complete removal of the InP substrate. In the long run, a flip-chip type of hybridization scheme that employs indium bonding comparable to that used in infrared FPA manufacturing would be a far more manufacturable way to integrate mixed material electronics. The indium bonding method also offers the advantage of reliably yielding low contact resistances, which is difficult for the Au-Au bonding in the baseline thin-film integration method used in this work when multiple pads must be contacted and the flatness of thin-film structure is imperfect. The drawback to hybridization by indium bonding, or any similar mixed-material hybridization, is a limitation in circuit speed for truly scaled RTDs due to interconnect parasitics.

8.3.2. Lateral and vertical scaling of the InAs/AlSb HEMT

The most obvious improvement to the baseline InAs/AlSb HEMT described in this work would be the reduction of the gate length from 0.2 μm to 0.1 μm or less. A 0.1 μm gate length should increase the InAs/AlSb HEMT's f_τ to at least 250 GHz. The increased f_τ, as was shown in Chapter 7, will lower the noise figure at high operating frequencies, where thermal noise is the dominant noise mechanism. In addition to reducing HEMT lateral dimension, a reduction in the barrier thickness would be expected to improve the transconductance, thereby increasing the power gain, albeit at the cost of

linearity. A moderate improvement in power gain would enable the realization of ultra-low power W-band LNAs operating at 94 GHz based on 0.1 μm InAs/AlSb HEMTs. While the further reduction in the HEMT barrier thickness from 180 Å is expected to cause an increase in the gate leakage current, this increase can be tolerated if it is not too large because the noise figure at W-band would be less sensitive to the gate leakage current than the noise figure at the lower frequencies (2-25 GHz) reported in Chapter 7.

8.3.3. Reliability and failure analysis of the InAs/AlSb HEMT

Before the InAs/AlSb HEMT can be transitioned into a production technology, a great deal of work needs to be done to determine its reliability over time and to understand its failure mechanisms. For example, preliminary experience has showed us that the "gate sinking" phenomenon [91]-[93], in which the gate metal progressively interdiffuses with the HEMT barrier under thermal or electrical stress, is the most common cause of device failure. While gate sinking is also the most prevalent failure mode in GaAs and InP-based HEMTs, the InAs/AlSb HEMT as described in this work suffers from this mode of degradation at relatively low temperatures and burn-in times. This effect may require substitution of the Ti/Pt/Au gate metal stack with a more thermally stable metallization using a refractory metal such as molybdenum at the metal-semiconductor contact, and experimentation along these lines is warranted. Finally, considering the early stage of development, long-term reliability testing of both discrete devices and MMICs will be essential to the advancement of the InAs/AlSb HEMT as a MMIC technology.

8.3.4. Development of a back-gated transferred substrate InAs/AlSb HEMT

Because it would eliminate the negative effects of impact-generated holes in the InAs/AlSb HEMT, namely high gate leakage currents and low drain-source impedance, a back-gated InAs/AlSb HEMT would represent the ultimate in the evolution of this HEMT technology. As discussed in Chapter 1, the back-gated HEMT is extremely challenging because it requires that the hole-collecting back-gate be scaled to nearly the same dimensions as the top gate in order to avoid a large shunt capacitance between the channel and back-gate. Additional challenges include the difficulties of removing the growth substrate and underlying epitaxial layers, aligning the back-gate, and developing the embedding transmission line environment. Nevertheless, if the metamorphic InAs/AlSb HEMT on GaAs reaches maturity, the benefits transferred-substrate HEMT would make it a worthwhile endeavor.

APPENDIX A

NEXT-GENERATION RTD PROCESS RUN SHEET

A.1. RTD Patterning

A.1.1 Clean Wafers

1. $NH_4OH:H_2O$ :: 1:1, 60 s
2. Spin rinse, spin dry

A.1.2 TiW Deposition

1. Argon back-sputter, 150 W, 30 s
2. Sputter 1000 Å TiW

A.1.3 Nitride Deposition

1. Deposit 2500 Å PECVD silicon nitride
2. Check thickness and refractive index with ellipsometer

A.1.4 RTD Photolithography

1. HMDS vapor prime
2. Spin ip3000-35 resist at 5 krpm for 60 s
3. Pre-bake 90°C for 60 s
4. Expose layer RTD 650 ms, blind step
5. Develop NMD-W (2.38% TMAH) 60 s, rinse 20 s
6. Inspect under microscope

A.1.5 Nitride Undercut

1. Slow rise on hotplate to 120°C
2. Descum in oxygen-argon plasma, 100 W, 30 s
3. Etch nitride in CF_4/O_2 plasma, 100 W, 2 min.
4. Slow rise on hotplate to 110°C
5. $HCl:H_2O$ :: 1:1, 30 s
6. Etch remaining nitride in BOE for 25 s or until clear
7. Water rinse, spin rinse, spin dry
8. Inspect under microscope for clearing and undercut

A.1.6 Emitter Metal Deposition and Liftoff

1. Evaporate Ti/Pt/Au/Ti, 400/400/3000/500 Å.
2. Soak in warm acetone until metal lifts
3. Stripper 106, Methanol, H_2O rinse

A.1.7 Remove TiW and Nitride from the Field

1. Plasmaquest downstream oxygen asher 500 W for 5 min.
2. Etch nitride and TiW in CF_4/O_2 RIE, 25 mT, 100 W, 30 min.
3. $HCl:H_2O$ :: 1:1, 30 s
4. H_2O_2 (30%) for 2 min.
5. Inspect under microscope

A.1.8 RTD Mesa Etching

1. Ion Mill for 6 min.

2. Clean up etch in H_2SO_4:H_2O_2:H_2O :: 1:8:160 for 10 s
3. Spin rinse, spin dry

A.1.9 Test Probable RTDs

A.2. Bottom Contact

A.2.1.. Deposit Passivation Nitride

1. Deposit 3000 Å PECVD silicon nitride
2. Check thickness and refractive index with ellipsometer

A.2.2. Ohmic Photolithography

1. HMDS vapor prime
2. Spin ip3000-35 resist at 6 krpm for 60 s
3. Pre-bake 90°C for 60 s
4. Expose layer OHMIC 650 ms, align to RTD
5. Develop NMD-W (2.38% TMAH) 60 s, rinse 20 s
6. Inspect under microscope

A.2.3. Nitride Etch and Undercut

1. Slow rise on hotplate to 120°C
2. Descum in oxygen/argon plasma, 50 W, 60 s
3. Etch nitride in CF_4/O_2 plasma, 50 W, 5 min.
4. Slow rise on hotplate to 110°C

5. $HCl:H_2O$ :: 1:1, 30 s
6. Etch remaining nitride in BOE for 60 s or until clear
7. Spin rinse, spin dry

A.2.4. Ohmic Metal Deposition and Liftoff

1. Argon back-sputter, 150 W, 30 s
2. Sputter 1000 Å TiW
3. Evaporate Ti/Pt/Au/Ti, 400/400/2500/200 Å.
4. Soak in warm acetone until metal lifts
5. Stripper 106, Methanol, H_2O rinse

A.3. Isolation Mesa

A.3.1. Clean wafers

1. Plasmaquest downstream oxygen asher 500 W for 5 min
2. $NH_4OH:H_2O$ :: 1:1, 60 s
3. Spin rinse, spin dry

A.3.2. Nitride Deposition

1. Deposit 400 Å PECVD silicon nitride
2. Check thickness and refractive index with ellipsometer

A.3.3. Isolation Mesa Photolithography

1. HMDS vapor prime

2. Spin Shipley 510 resist at 5 krpm for 30 s
3. Pre-bake 90°C for 60 s
4. Expose layer NMESA 400 ms, align to RTD
5. Develop NMD-W (2.38% TMAH) 75 s, rinse 20 s
6. Inspect under microscope

A.3.4. Nitride Etch

1. Oven bake at 140°Cfor 20 min.
2. Descum in oxygen/argon plasma, 50 W, 60 s
3. Etch nitride in CF_4/O_2 RIE, 25 mT, 100 W, 10 min.

A.3.5. Isolation Mesa Etch

1. Slow rise on hotplate to 120°C
2. Ion mill wafers 15 min. to etch 4500-5000 Å.
3. Wet etch in H_2SO_4:H_2O_2:H_2O :: 1:8:160 for 25 s
4. Spin rinse, spin dry

A.3.6. Strip Photoresist

1. Plasmaquest downstream oxygen asher 500 W for 5 min
2. Stripper 106, Methanol, H_2O rinse
3. Plasmaquest downstream oxygen asher 500 W for 2 min

A.4. Oxide Deposition and Via1 Etching

A.4.1. Clean Wafers

1. High pressure water spray
2. $NH_4OH:H_2O$ :: 1:1, 60 s
3. Spin rinse, spin dry

4.2. Nitride Deposition

4. Deposit 400 Å PECVD silicon nitride
5. Check thickness and refractive index with ellipsometer

A.4.3. Spin-on Glass Deposition

1. High pressure water spray
2. Spin spin-on glass at 3 krpm
3. Slow rise on hotplate to 150°C
4. Vacuum bake at 300 C for 180 min.

A.4.4. PECVD Oxide Deposition

1. Deposit 400 Å PECVD silicon oxide
2. Check thickness and refractive index with ellipsometer

A.4.5. Via1 Photolithography

1. HMDS vapor prime
2. Spin ip3000-35 resist at 6 krpm for 60 s
3. Pre-bake 90°C for 60 s

4. Expose layer VIA1 650 ms, align to RTD
5. Develop NMD-W (2.38% TMAH) 60 s, rinse 20 s
6. Inspect under microscope

A.4.6. Via1 Etching

1. Slow rise on hotplate to 140 C
2. Oven bake at 100°C for 30 min.
3. Descum in oxygen/argon plasma, 50 W, 60 s
4. Etch oxide in CHF_3/O_2 RIE, 50 mT, 200 W, 60 min
5. Inspect under microscope

A.4.7. Strip Photoresist

1. Plasmaquest downstream oxygen asher 500 W for 5 min
2. Stripper 106, Methanol, H_2O rinse
3. Plasmaquest downstream oxygen asher 500 W for 2 min

A.5. First Metal

A.5.1. Sputter Metal1

1. Argon back-sputter, 150 W, 180 s
2. Sputter TiW/Au/TiW, 1500/4000/400 Å

A.5.2. Metal1 Photolithography

1. HMDS vapor prime

2. Spin Shipley 510 resist at 2.5 krpm for 30 s
3. Pre-bake 90°C for 60 s
4. Expose layer METAL1 400 ms, align to RTD
5. Develop NMD-W (2.38% TMAH) 75 s, rinse 20 s
6. Inspect under microscope

A.5.3. Metal1 Etching

1. Slow rise on hotplate to 140 C
2. Oven bake at 100°C for 30 min.
3. Descum in oxygen/argon plasma, 100 W, 30 s
4. Etch TiW in CF_4/O_2 RIE, 25 mT, 100 W, 5 min.
5. Ion mill gold for 12 min. or until gold clears
6. Etch TiW in CF_4/O_2 RIE, 25 mT, 100 W, 15 min
7. Probe to ensure metal has cleared from field

A.5.4. Strip Photoresist

1. Plasmaquest downstream oxygen asher 500 W for 5 min
2. Stripper 106, Methanol, H_2O rinse
3. Plasmaquest downstream oxygen asher 500 W for 2 min

A.6. BCB Deposition and Via2 Etching

A.6.1. Wafer Preparation and Nitride Deposition

1. High pressure water spray

2. Spin rinse, spin dry
3. Deposit 400 Å PECVD silicon nitride
4. Check thickness and refractive index with ellipsometer

A.6.2. Spin BCB Polymer

1. Bake on hotplate at 120°C for 60 s
2. Spin AP3000 primer at 5 krpm for 20 s
3. Spin Cyclotene 3022-46 at 5 krpm for 30 s (~2.3 μm thickness)
4. Back-side rinse with mesitylene
5. Slow rise to 100 C on hotplate

A.6.3. Cure BCB

1. Load wafers in Blue M oven with continuous N_2 purge
2. High flow N_2 purge at 50°C for 27 min.
3. Ramp to 100°C at 3°C/min.
4. Soak at 100°C for 20 min.
5. Ramp to 150°C at 3°C/min.
6. Soak at 150°C for 20 min.
7. Ramp to 260°C at 3°C/min.
8. Soak at 260°C for 50 min.
9. Natural cool down

A.6.4. Sputter Via2 Etch Mask

1. Argon back-sputter, 150 W, 60 s
2. Sputter TiW, 1000 Å

A.6.5. Via2 Photolithography

1. HMDS vapor prime
2. Spin ip3000 resist at 5 krpm for 30 s
3. Pre-bake 90°C for 60 s
4. Expose layer VIA2 500 ms, align to METAL1
5. Develop NMD-W (2.38% TMAH) 65 s, rinse 20 s
6. Inspect under microscope

A.6.6. Via2 Etching

1. Bake on hotplate at 120°C for 60 s
2. Descum in oxygen/argon plasma, 100 W, 30 s
3. Etch TiW in CF_4/O_2 RIE, 25 mT, 100 W, 10 min.
4. Etch BCB in O_2/CF_4 RIE, 50/12 sccm, 150 mT, 200 W, 15 min. or until clear
5. Inspect under microscope
6. Etch nitride in CF_4/O_2 RIE, 25 mT, 100 W, 4 min.
7. Inspect under microscope

A.7. Second Metal

A.7.1. Sputter Metal2

1. Argon back-sputter, 150 W, 120 s
2. Sputter TiW/Au/TiW, 1500/6000/400 Å

A.7.2. Metal2 Photolithography

1. HMDS vapor prime
2. Spin Shipley 510 resist at 2.5 krpm for 30 s
3. Pre-bake 90°C for 60 s
4. Expose layer METAL2 400 ms, align to METAL1
5. Develop NMD-W (2.38% TMAH) 60 s, rinse 20 s
6. Inspect under microscope

A.7.3. Metal2 Etching

1. Slow rise on hotplate to 140 C
2. Oven bake at 100°C for 30 min.
3. Descum in oxygen/argon plasma, 100 W, 30 s
4. Etch TiW in CF_4/O_2 RIE, 25 mT, 100 W, 5 min.
5. Ion mill gold for 15 min. or until gold clears
6. Etch TiW in CF_4/O_2 RIE, 25 mT, 100 W, 5 min
7. Etch remaining TiW in H_2O_2 for 5 min or until TiW clears
8. Probe to ensure metal has cleared from field

A.7.4. Strip Photoresist

1. Stripper 106, Methanol, H_2O rinse
2. Inspect under microscope

A.8. ELO Structure Isolation

A.8.1. Etch Mask Deposition

1. Argon back-sputter, 150 W, 30 s
2. Sputter TiW, 250 Å
3. Evaporate Al, 1000 Å

A.8.2. ELO Isolation Photolithography

1. HMDS vapor prime
2. Spin Shipley 510 resist at 2.5 krpm for 30 s
3. Pre-bake 90°C for 60 s
4. Expose layer ELO 400 ms, align to METAL1
5. Develop NMD-W (2.38% TMAH) 60 s, rinse 20 s
6. Inspect under microscope

A.8.3. Etch Metal Mask

1. Bake on hotplate at 140°C for 60 s
2. Descum in oxygen/argon plasma, 100 W, 30 s
3. Etch 1000 Å Al in heated aluminum leach etchant
4. H_2O rinse
5. Spin rinse, spin dry
6. Etch TiW in CF_4/O_2 RIE, 25 mT, 100 W, 2 min.
7. Inspect under microscope

A.8.4. Etch BCB and Oxide

1. Etch BCB in O_2/CF_4 RIE, 50/12 sccm, 150 mT, 200 W, for 25 min. or until clear
2. Etch oxide in CHF_3/O_2 RIE, 50 mT, 200 W, 60 min or until clear, over-etch is acceptable

A.8.5. Strip Metal Mask

1. Etch 1000 Å Al in heated aluminum leach etchant
2. H_2O rinse
3. Etch TiW in H_2O_2, 3 min.
4. Inspect under microscope

APPENDIX B

YIELD AND UNIFORMITY OF NEXT GENERATION RTDS FOR THIN-FILM INTEGRATION

B.1. Introduction

This appendix is included for the interested reader to supplement the basic yield and uniformity data of the next generation scaled RTDs presented in Section 4.3. The content is comprised of the results of wafer mapping of the DC current-voltage characteristics of the discrete RTDs of each of the four device areas included on the mask. The data presented in this appendix was measured with the intent of gauging the overall device yield and validating the fabrication process. It is not intended as a full analysis of the device level uniformity and the causes thereof.

There were three wafers included in this lot, Wafers 4241, 4242, and 4243, with targeted peak current densities of 4, 30, and 60 kA/cm^2, respectively. The wafer mapping consisted of a DC voltage sweep between −1 V and +1 V of a two-terminal front-contacted RTD. One RTD each of nominal area 1.4 × 1.4 μm, 2 × 2 μm, 4 × 4 μm, and 6 x 6 μm^2 was measured in each 10 × 10 mm field on each of the three-inch wafers. There was no significant difference in the fundamental trends visible in the measured device electrical parameters, and the device yields were similar on all three wafers.

The results of the yield and uniformity testing are divided into three sections. First, Section B.2 presents the device level yield of each of the four different RTDs on each wafer. Full wafer maps of the peak current and peak-to-valley current ratio (PVCR)

comprise are included in Section B.3. Lastly, Section B.4 covers the statistical distribution of the RTD parameters for each device area.

B.2. RTD Yield

The yield for all three wafers was very high. In fact, the excluding the 1.4×1.4 μm^2 RTDs, the yield was 100%, with the lone exception of a single 4×4 μm^2 RTD from the edge of Wafer 4242 which had a high valley current, approximately twice that of the typical RTD from this wafer. (It is also worth noting that this RTD had the largest peak current of the 4×4 μm^2 RTDs measured on this wafer.) When the non-edge fields are considered, every device larger than the minimum geometry RTD yielded. The 1.4×1.4 μm^2 RTDs had more modest yield, specifically 21 out of 22 for Wafer 4242, 31 of 32 for Wafer 4242, and 27 of 32 for wafer 4243. The most common failure was a short between terminals, with no negative differential resistance observable. On wafers 4241 and 4242, an additional RTD failed due to an anomalously high valley current. Figures B.1-B.3 show the overlaid DC I-V data for each of the three wafers. The relative uniformity of the non-edge fields with respect the entire wafer is apparent in Figures B.4-B.6, which show the same data with the edge fields excluded.

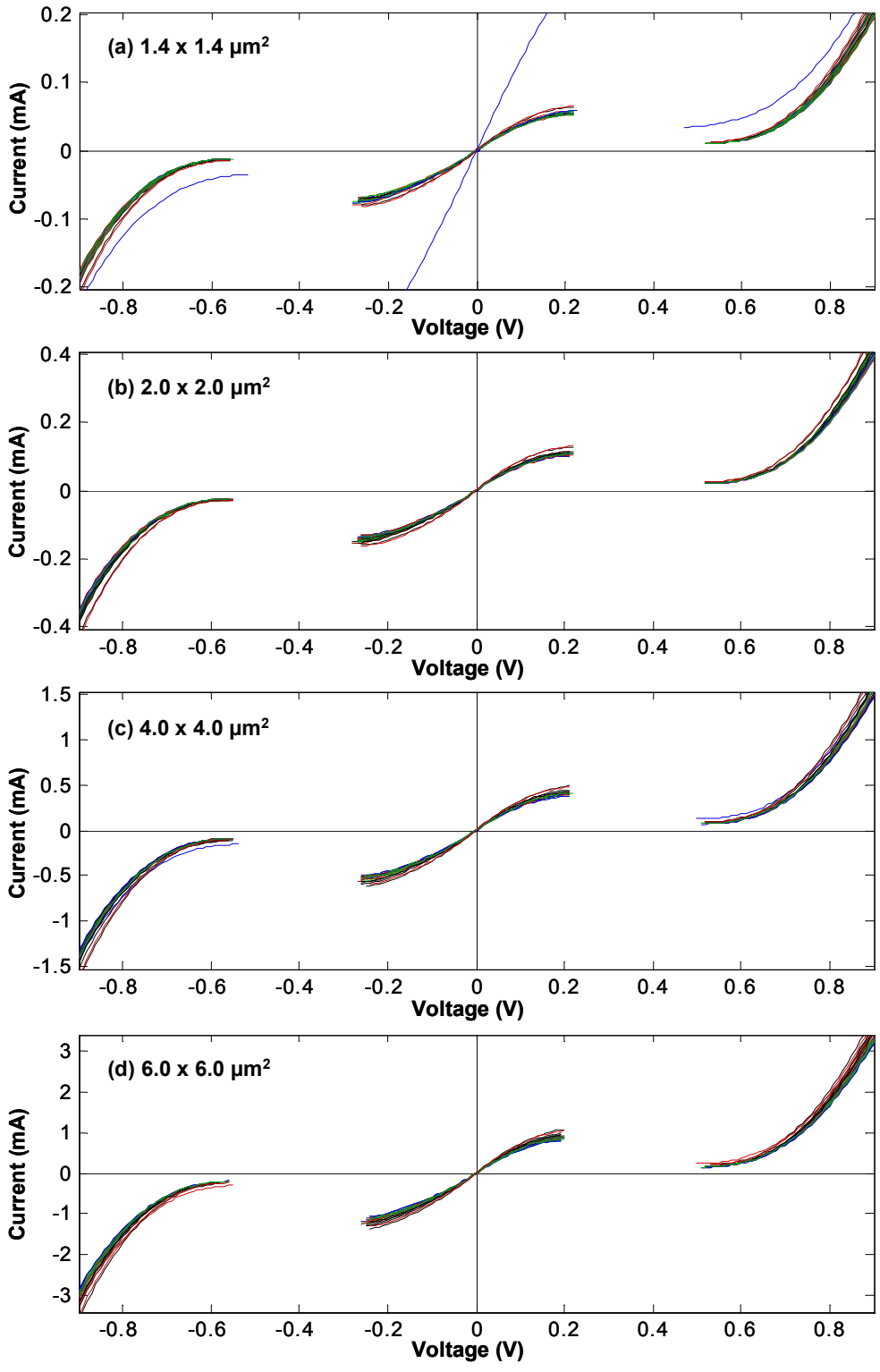


Figure B.1 All measured RTD I-V characteristics from Wafer 4241 for devices with area (a) 1.4 × 1.4 μm^2, (b) 2 × 2 μm^2, (c) 4 × 4 μm^2, and (d) 6 × 6 μm^2.

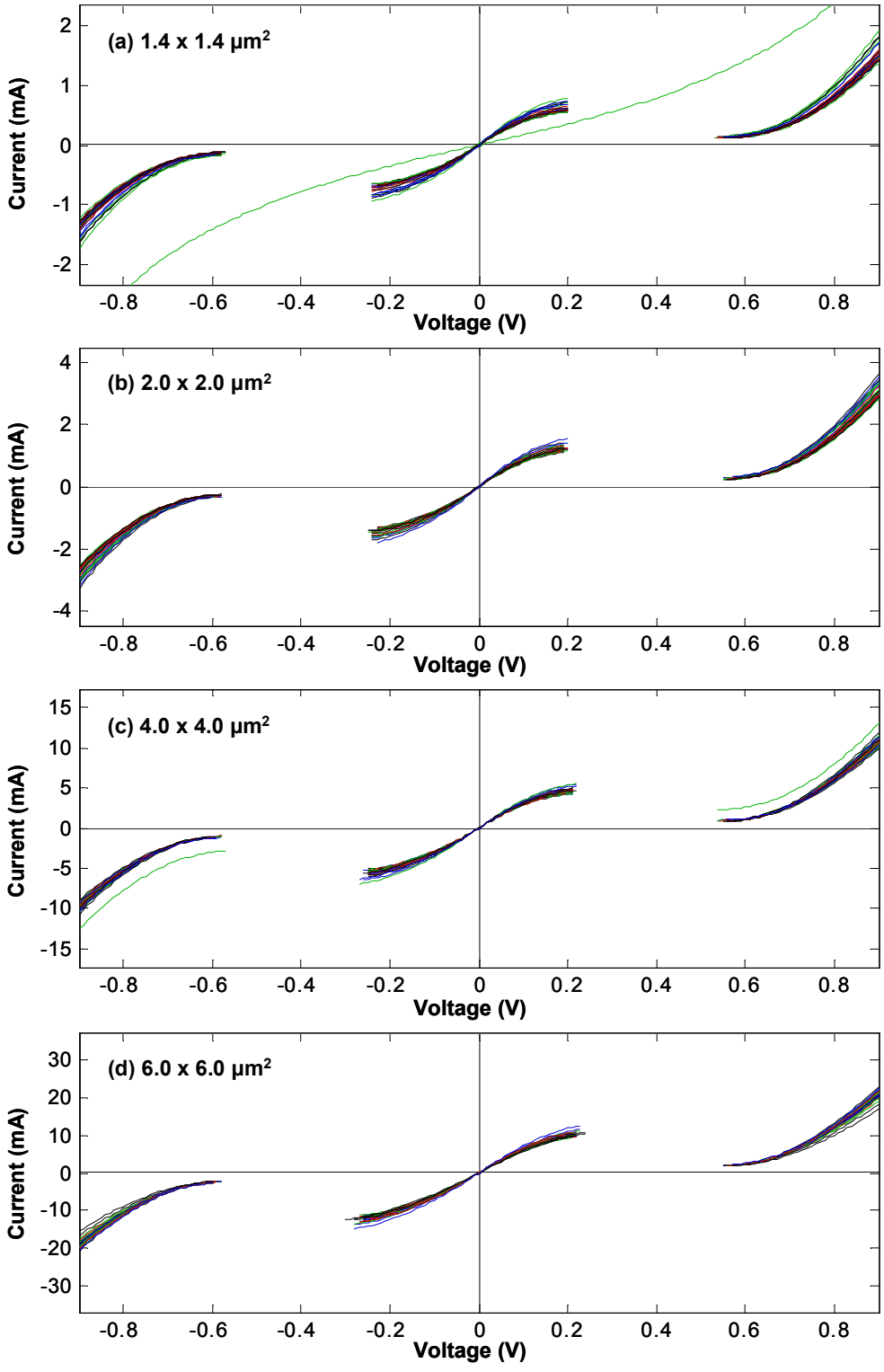


Figure B.2 All measured RTD I-V characteristics from Wafer 4242 for devices with area (a) 1.4 × 1.4 μm^2, (b) 2 × 2 μm^2, (c) 4 × 4 μm^2, and (d) 6 × 6 μm^2.

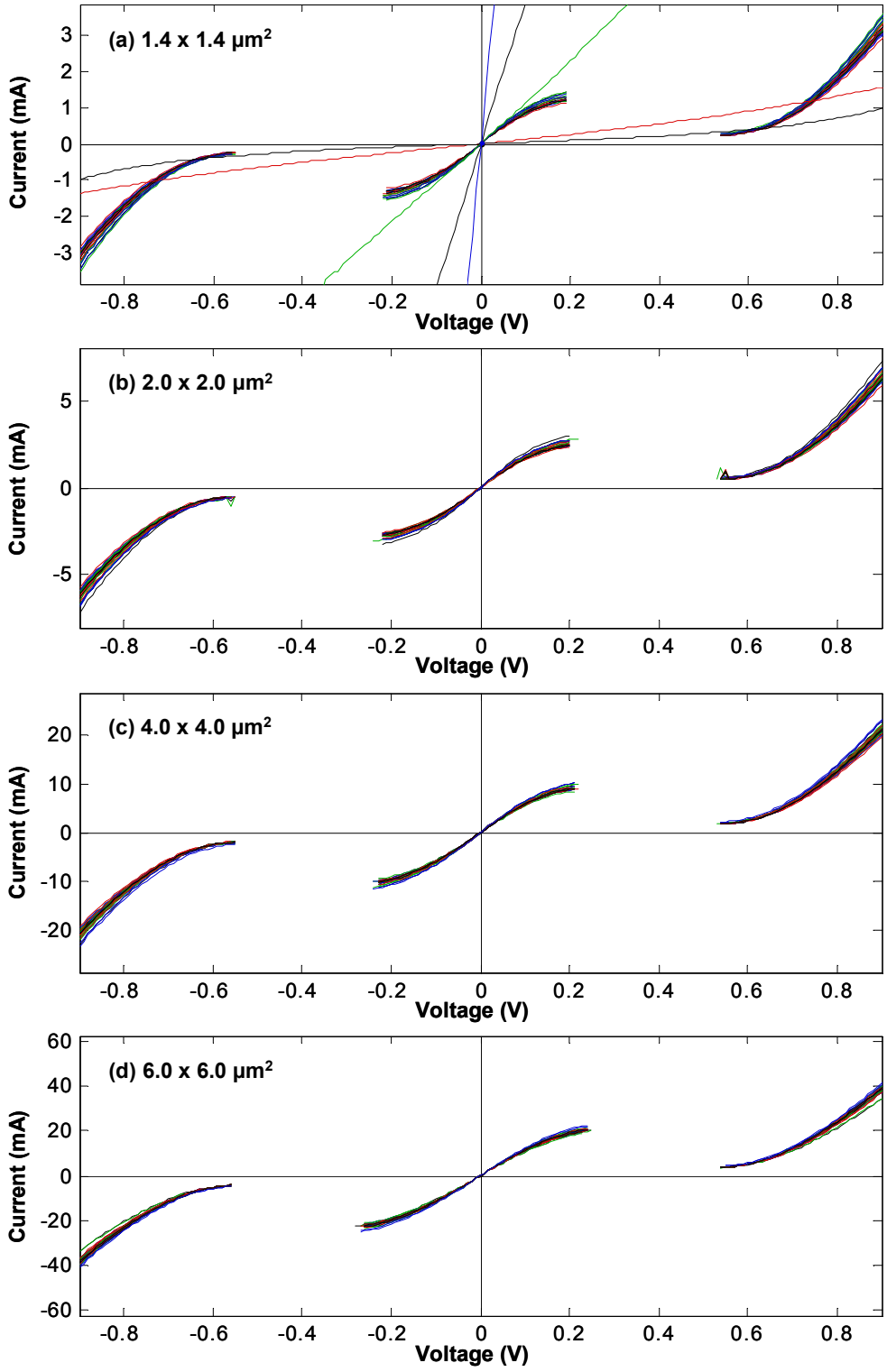


Figure B.3 All measured RTD I-V characteristics from Wafer 4243 for devices with area (a) 1.4 × 1.4 μm^2, (b) 2 × 2 μm^2, (c) 4 × 4 μm^2, and (d) 6 × 6 μm^2.

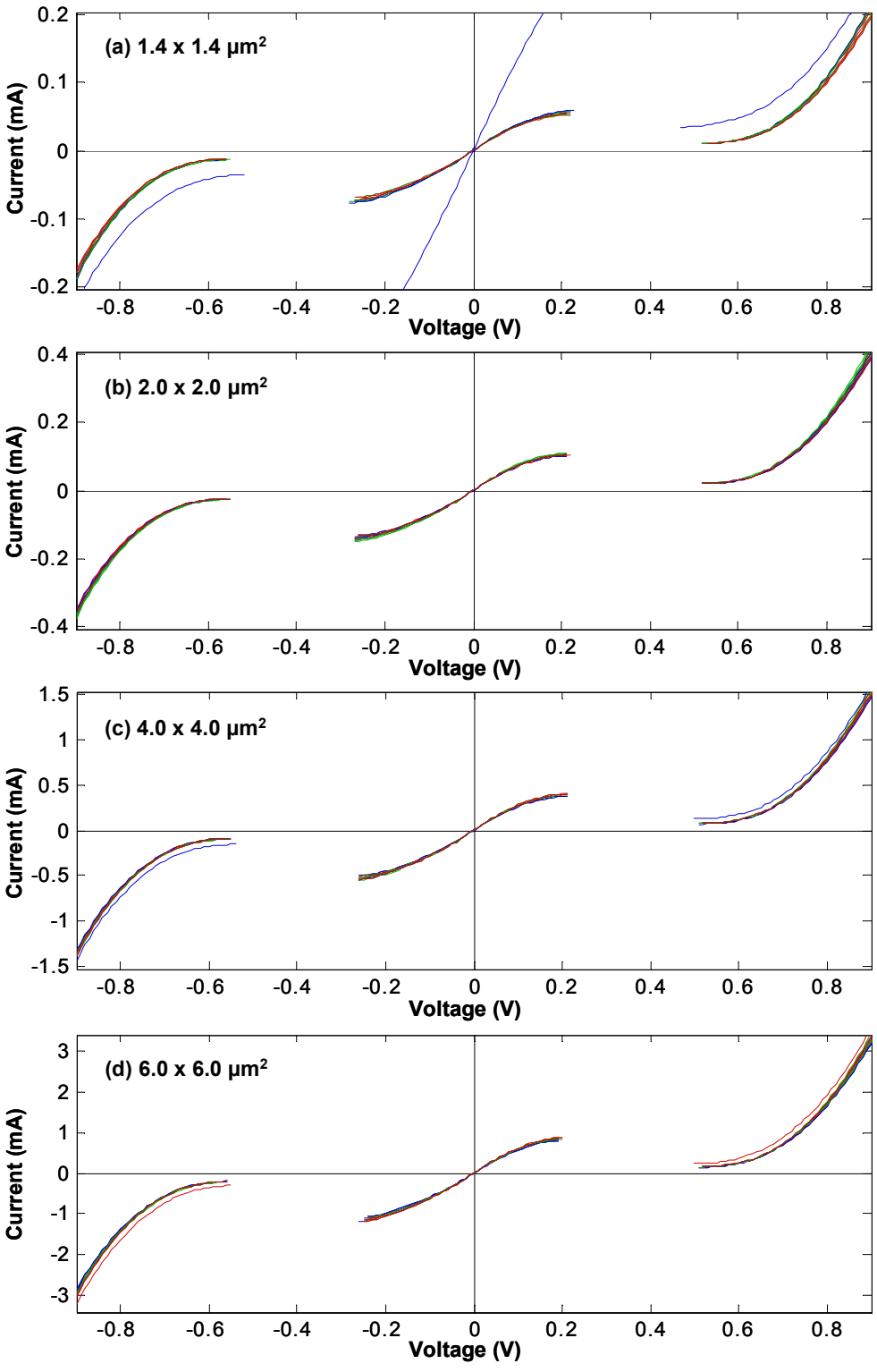


Figure B.4 Measured RTD I-V characteristics from non-edge fields of Wafer 4241 for devices with area (a) 1.4 × 1.4 μm^2, (b) 2 × 2 μm^2, (c) 4 × 4 μm^2, and (d) 6 × 6 μm^2.

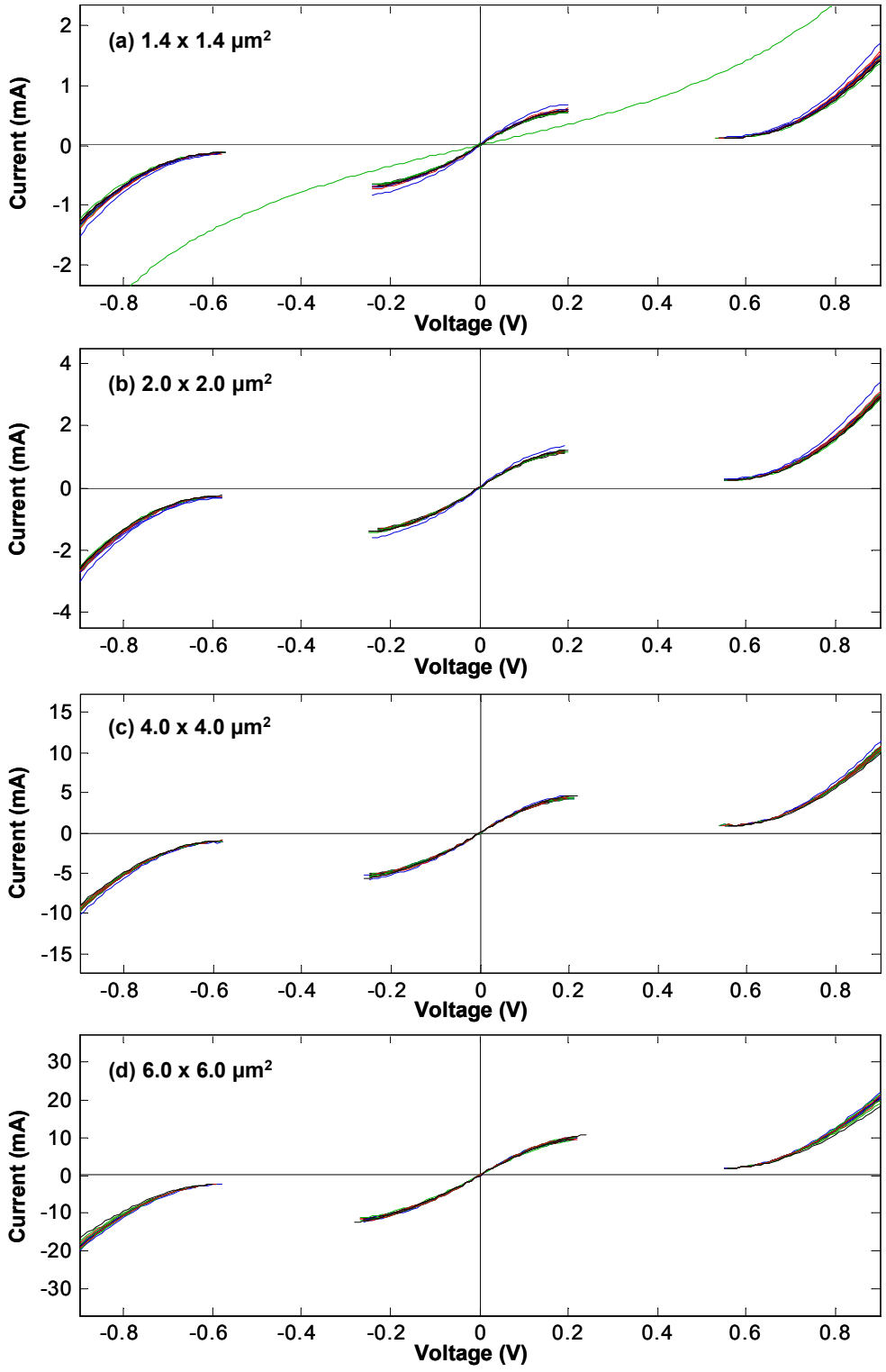


Figure B.5 Measured RTD I-V characteristics from non-edge fields of Wafer 4242 for devices with area (a) 1.4 × 1.4 μm^2, (b) 2 × 2 μm^2, (c) 4 × 4 μm^2, and (d) 6 × 6 μm^2.

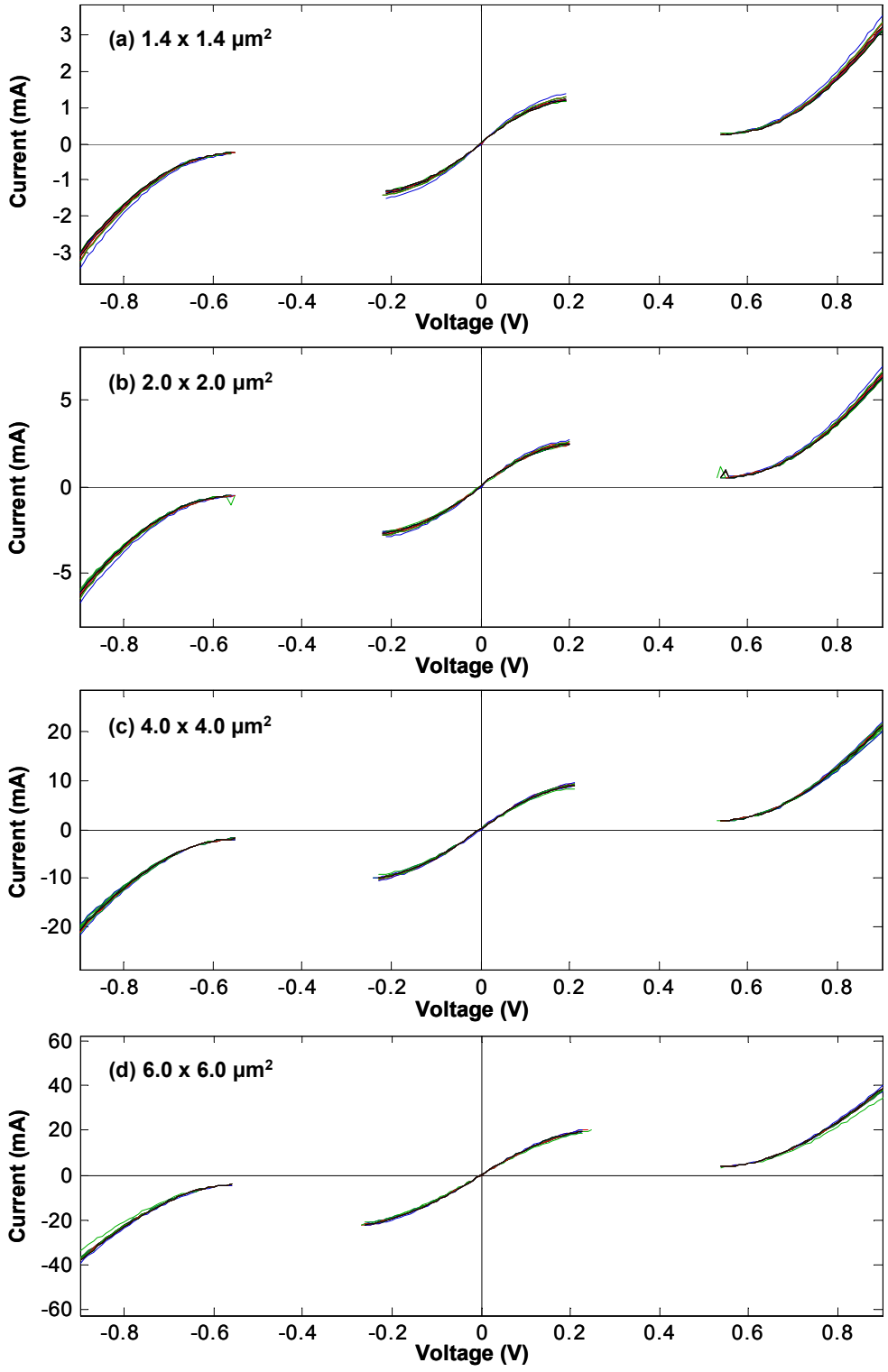


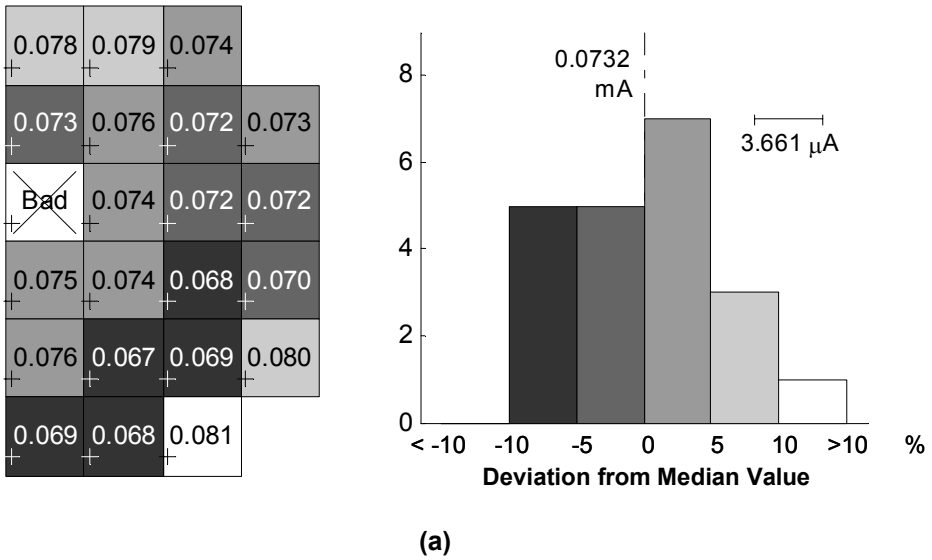
Figure B.6. Measured RTD I-V characteristics from non-edge fields of Wafer 4243 for devices with area (a) 1.4 × 1.4 μm^2, (b) 2 × 2 μm^2, (c) 4 × 4 μm^2, and (d) 6 × 6 μm^2.

B.3. RTD Uniformity and Wafer Maps

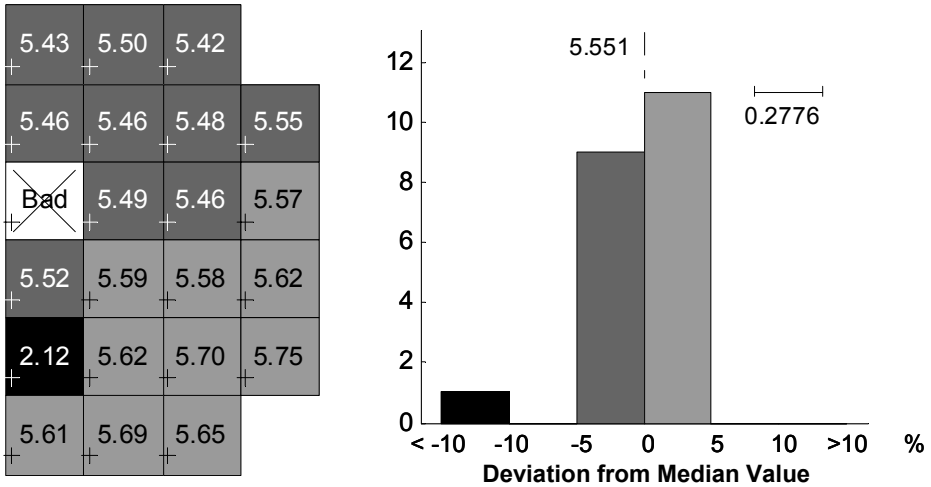
The figures in this section are devoted to the uniformity of the peak current and PVCR because they are the two parameters of prime importance, and because the variation in the peak and valley voltages was typically less than the measurement voltage resolution of 10 mV.

Figures B.7-B.10 show the wafer maps of the peak current and PVCR for the four different RTD areas from Wafer 4241. The RTD peak current clearly increases with proximity to the edge of the wafer, with the devices closest to the edge exhibiting approximately 25% higher peak current than those near the center of the wafer. As mentioned in Section 4.3, this effect is attributable to minor radial flux non-uniformity in the MBE growth system. If the experimental value of $-0.70\ \text{decade}/\text{nm}$ for the sensitivity of the peak current density to barrier thickness is used, then a 25% shift in the peak current density corresponds to a deviation in the barrier thicknesses of only 1.4 Å.

An equivalent pattern is observable in Figures B.11-B.14 and Figures B.15-B.18, which are the corresponding wafer maps for wafers 4242 and 4243, respectively. There is no definitive correlation between PVCR and position on the wafer, or does PVCR appear to be related to the RTD peak current. In wafers 4241 and 4242 there does appear to be a gradual linear increase in PVCR from one side of the wafer to the next, but the cause of this phenomenon is not known.

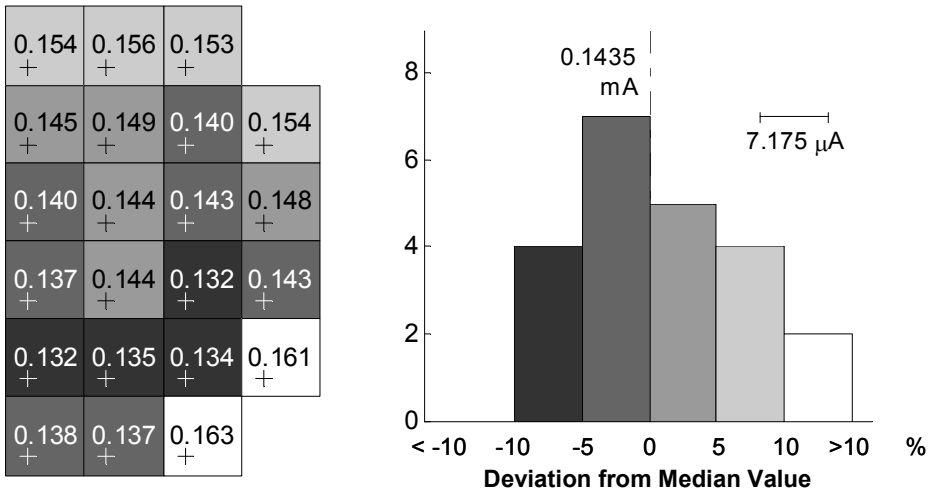


(a)

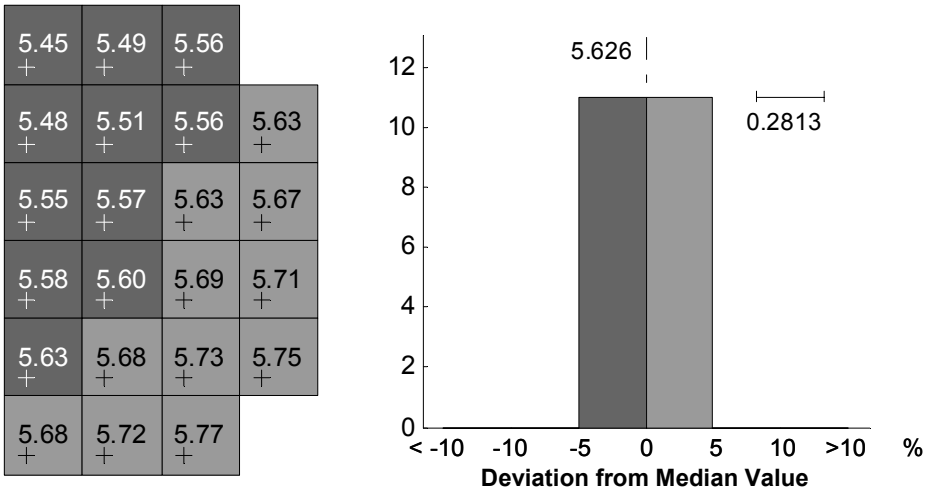


(b)

Figure B.7 Wafer map and distribution of (a) peak current (mA) and (b) PVCR for RTDs from Wafer 4241 with area $1.4 \times 1.4\ \mu m^2$.

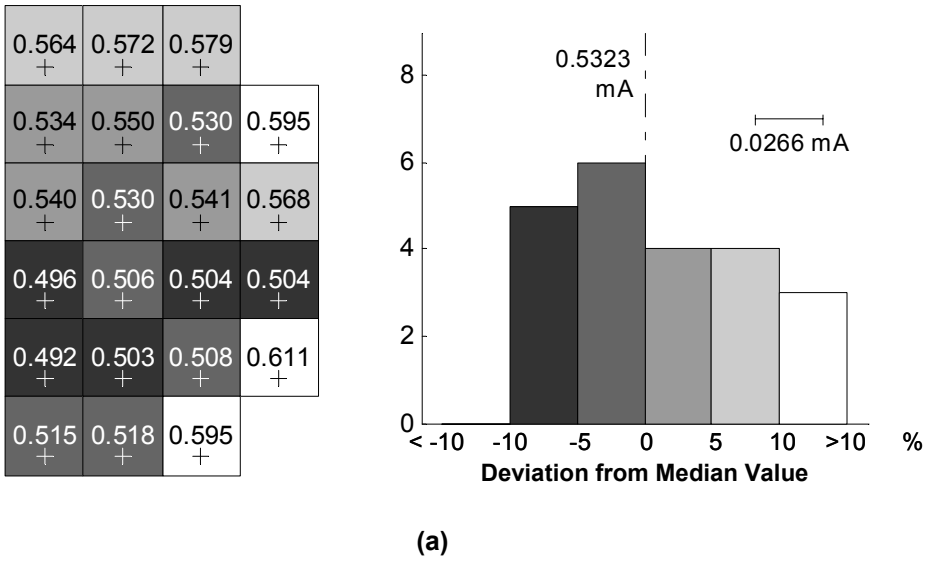


(a)

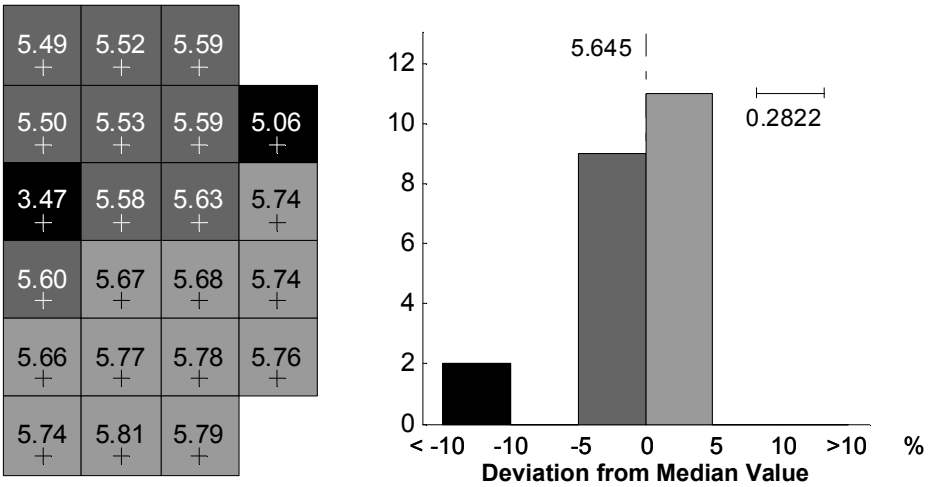


(b)

Figure B.8 Wafer map and distribution of (a) peak current (mA) and (b) PVCR for RTDs from Wafer 4241 with area $2 \times 2\ \mu m^2$.

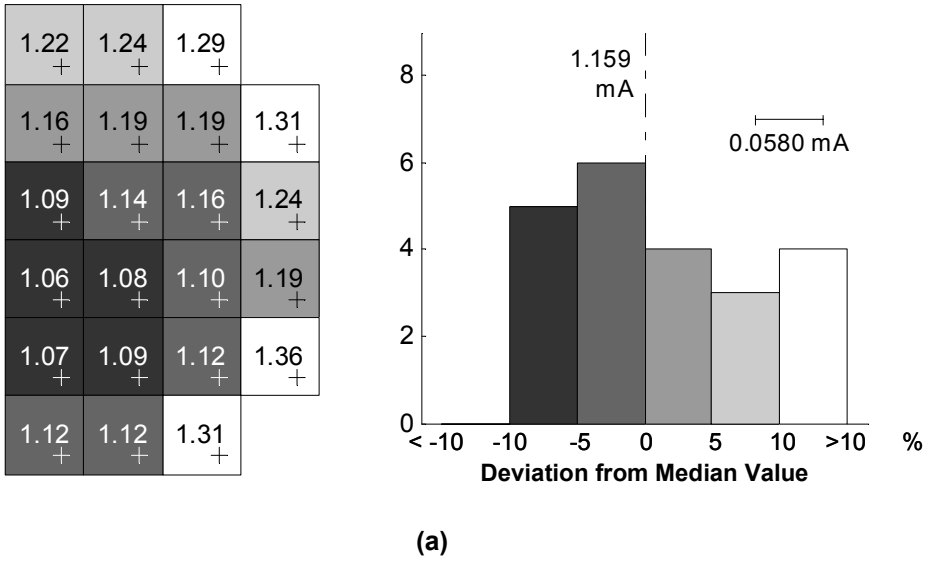


(a)

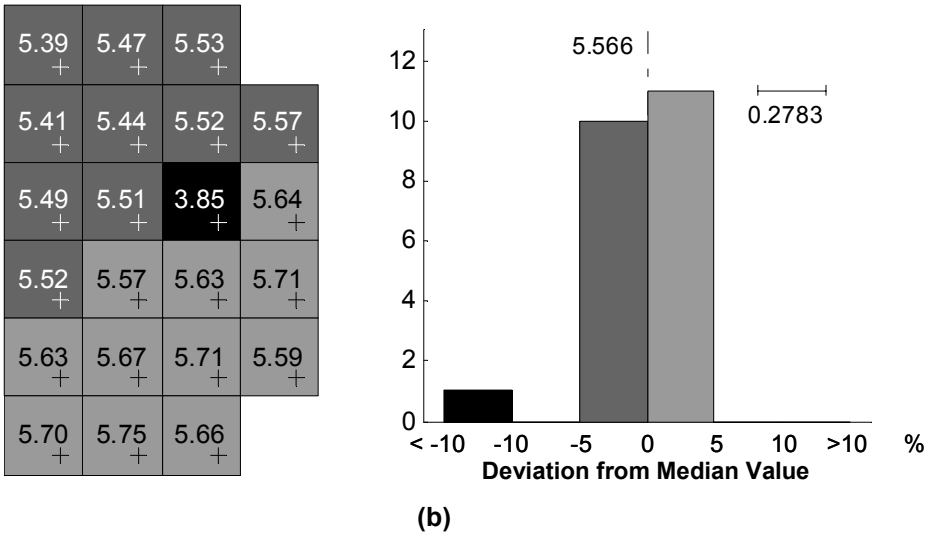


(b)

Figure B.9 Wafer map and distribution of (a) peak current (mA) and (b) PVCR for RTDs from Wafer 4241 with area $4 \times 4\ \mu m^2$.

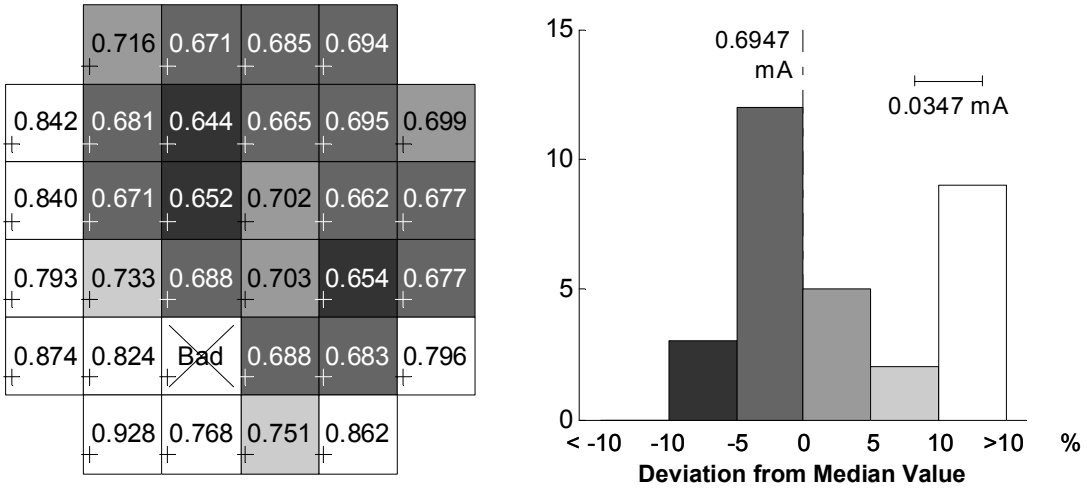


(a)

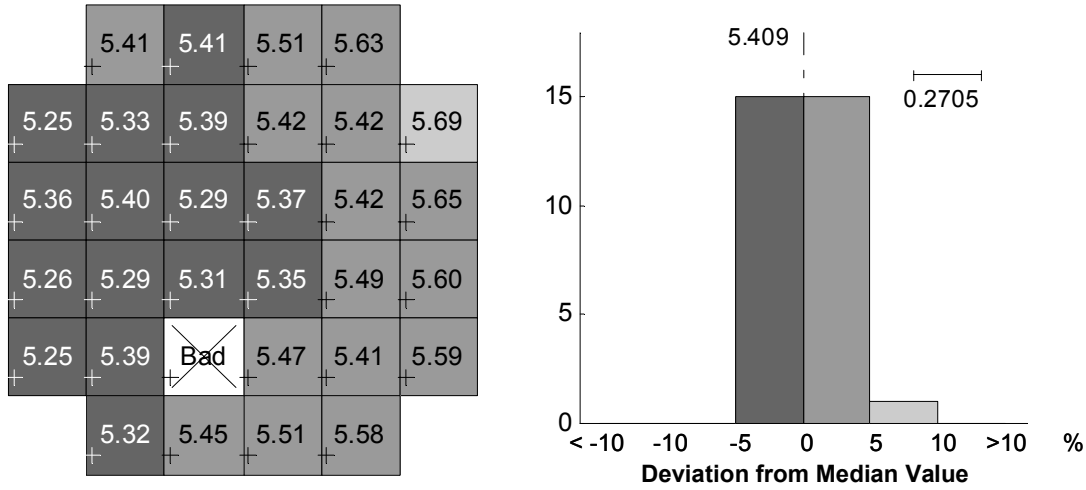


(b)

Figure B.10 Wafer map and distribution of (a) peak current (mA) and (b) PVCR for RTDs from Wafer 4241 with area $6 \times 6\ \mu m^2$.

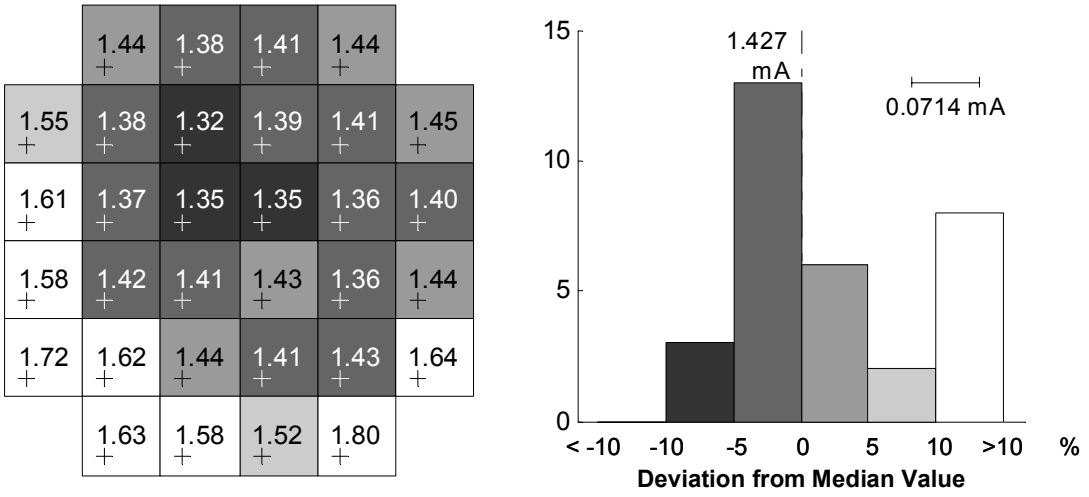


(a)

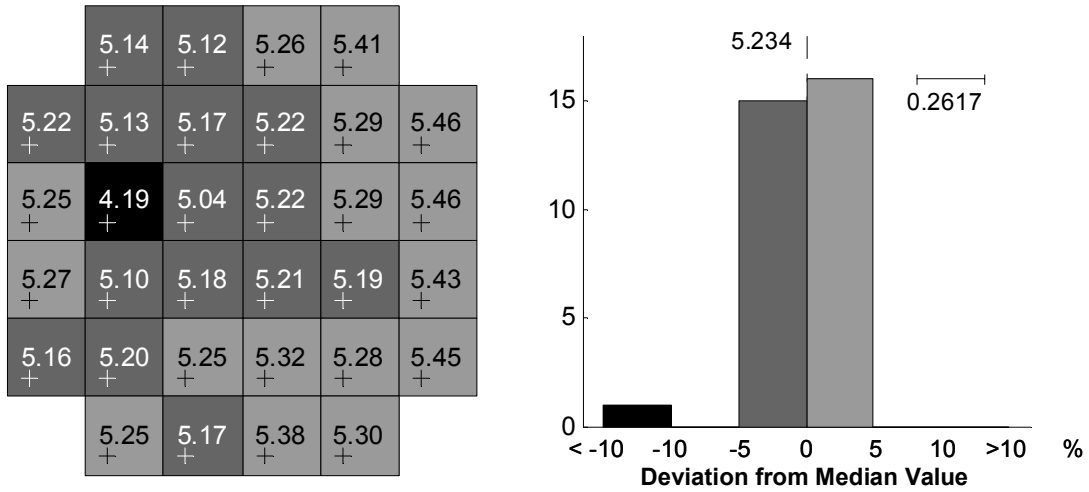


(b)

Figure B.11 Wafer map and distribution of (a) peak current (mA) and (b) PVCR for RTDs from Wafer 4242 with area $1.4 \times 1.4\ \mu m^2$.

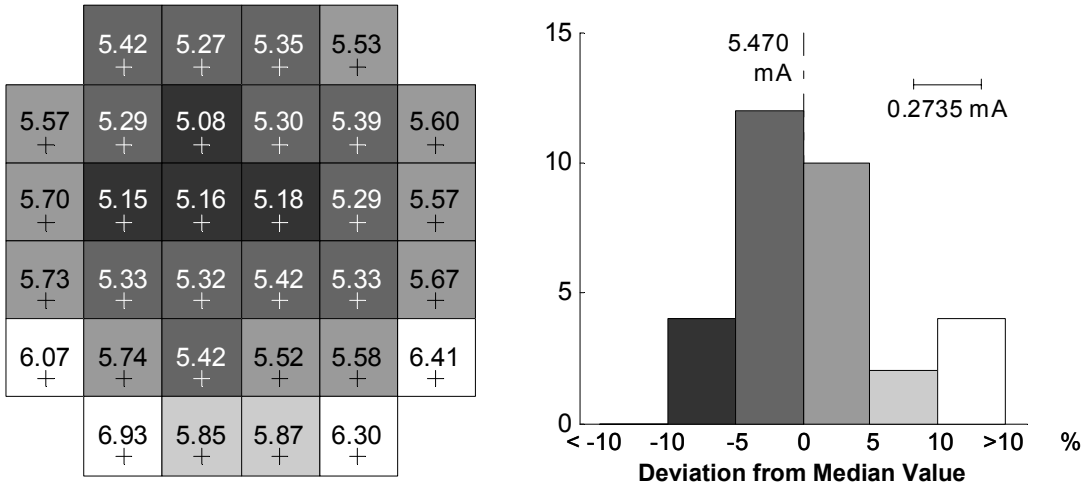


(a)

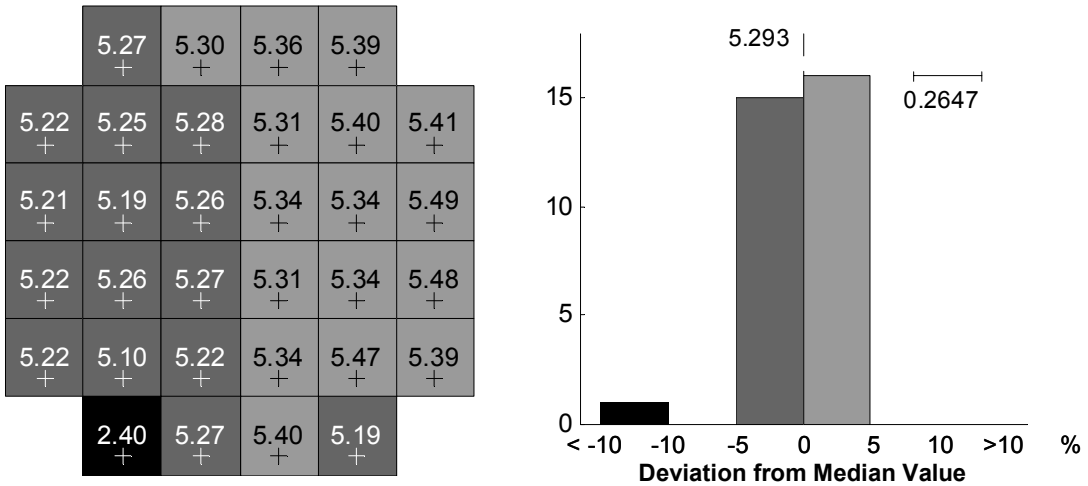


(b)

Figure B.12 Wafer map and distribution of (a) peak current (mA) and (b) PVCR for RTDs from Wafer 4242 with area $2 \times 2\ \mu m^2$.

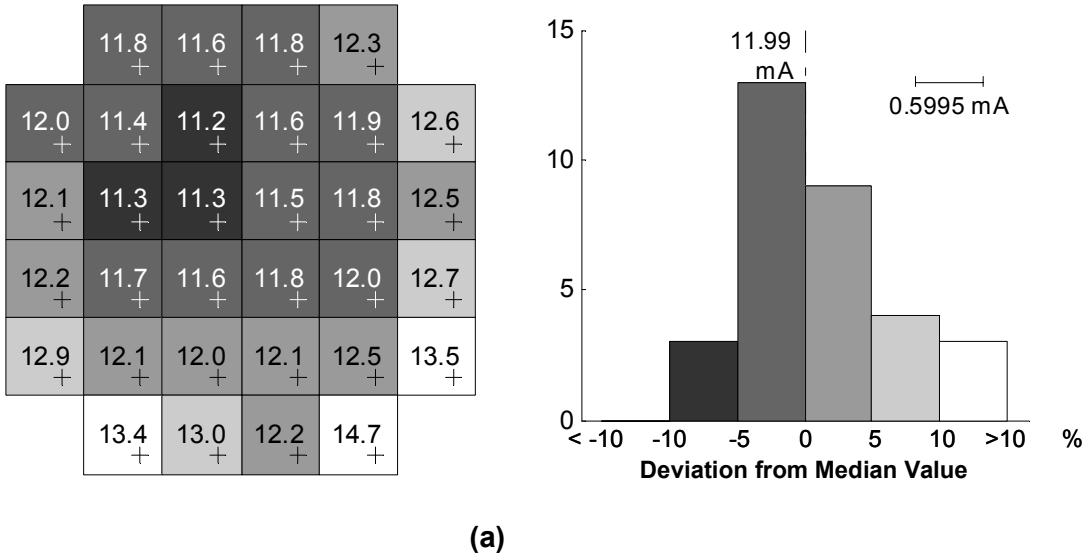


(a)

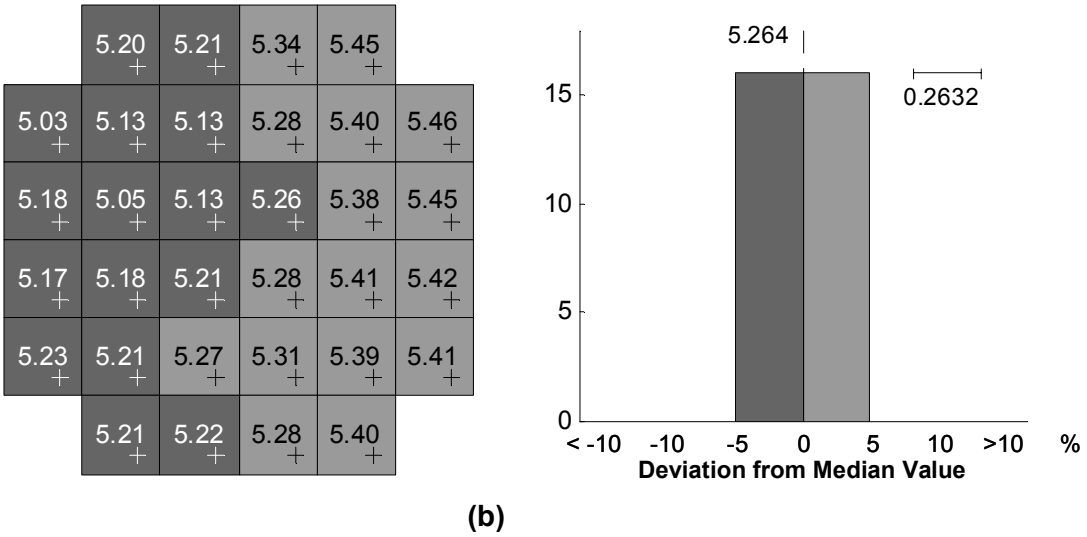


(b)

Figure B.13 Wafer map and distribution of (a) peak current (mA) and (b) PVCR for RTDs from Wafer 4242 with area $4 \times 4\ \mu m^2$.

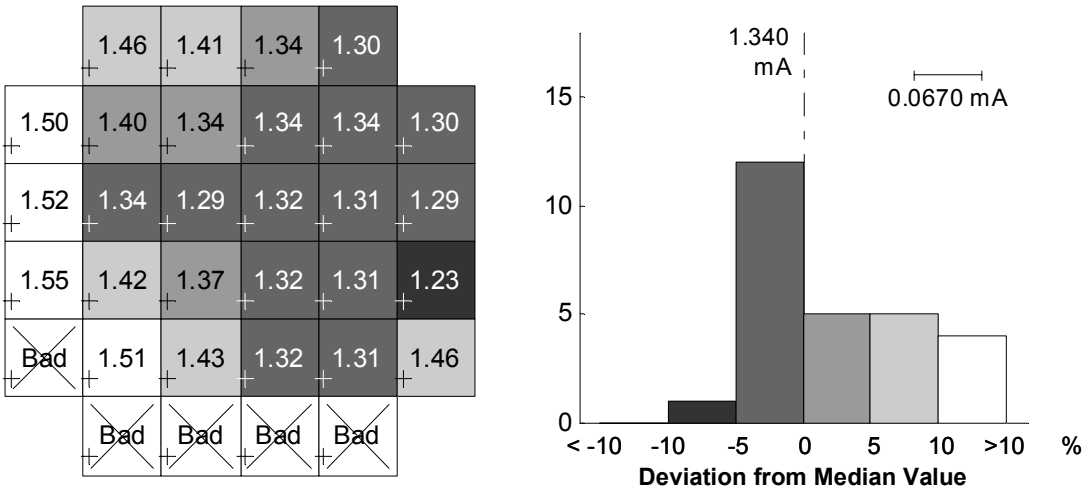


(a)

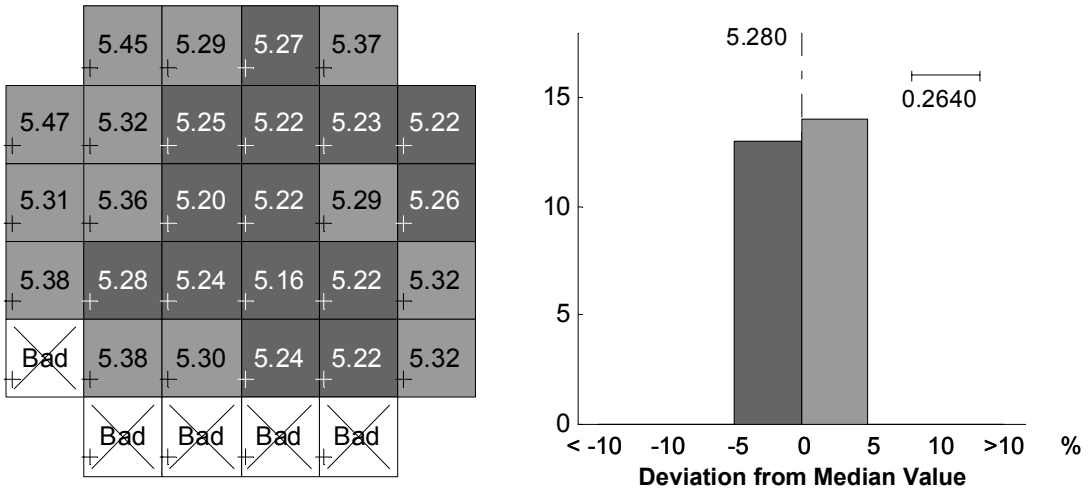


(b)

Figure B.14 Wafer map and distribution of (a) peak current (mA) and (b) PVCR for RTDs from Wafer 4242 with area $6 \times 6\ \mu m^2$.

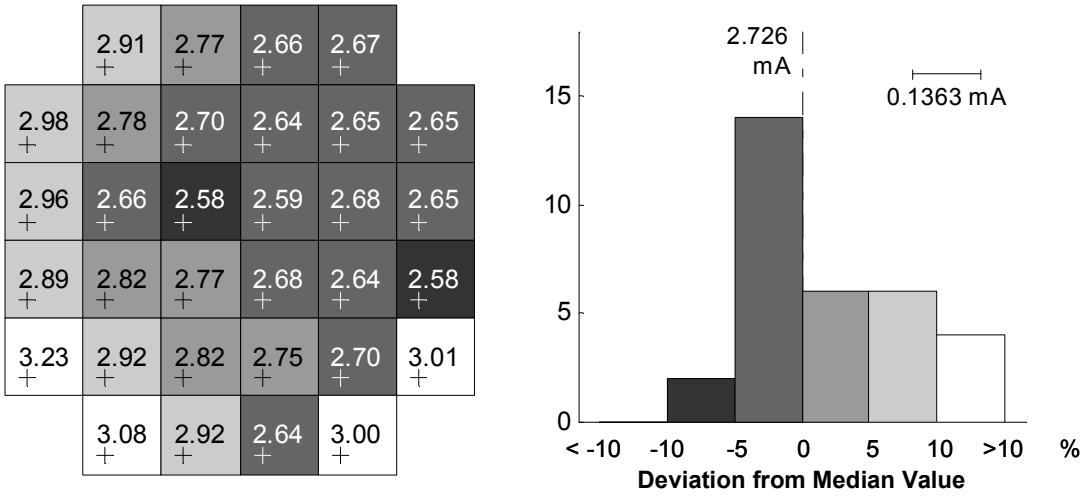


(a)

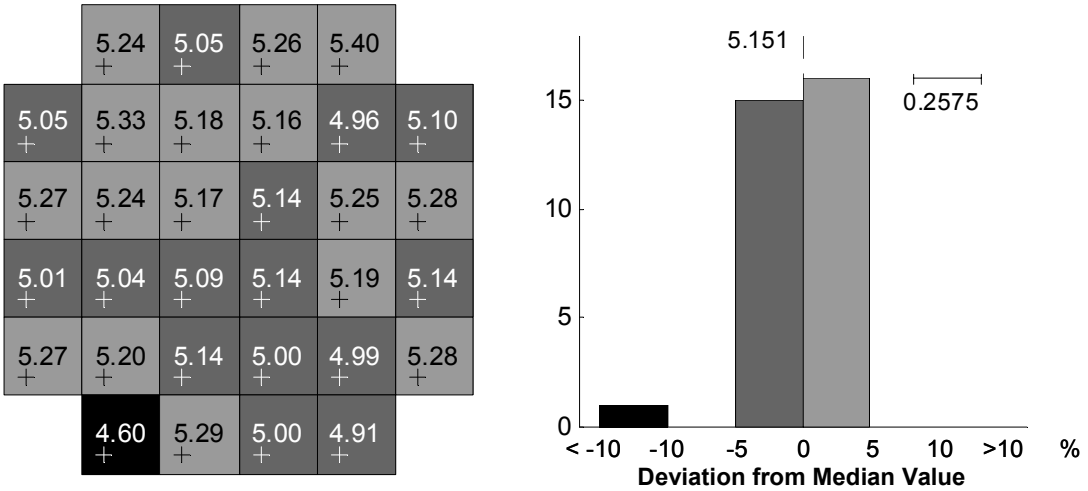


(b)

Figure B.15 Wafer map and distribution of (a) peak current (mA) and (b) PVCR for RTDs from Wafer 4243 with area $1.4 \times 1.4\ \mu m^2$.

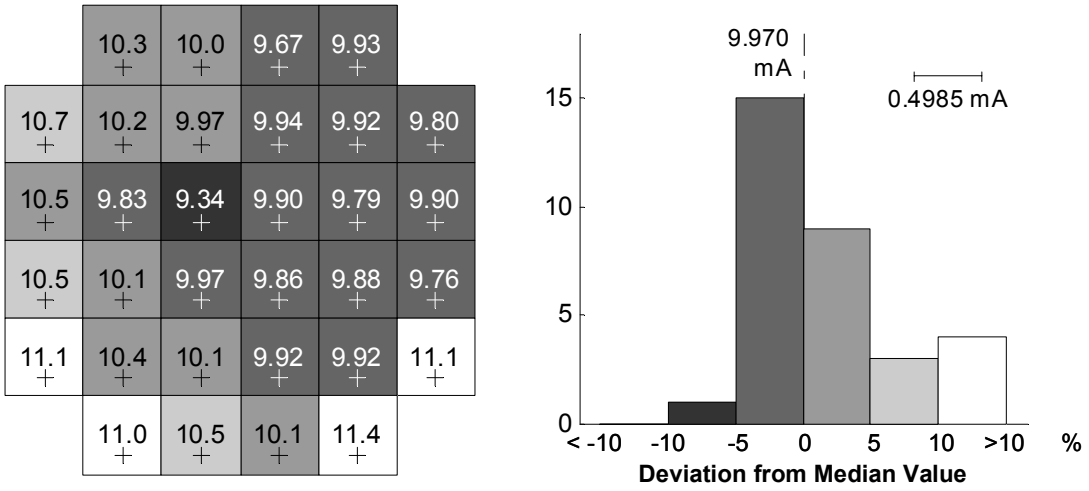


(a)

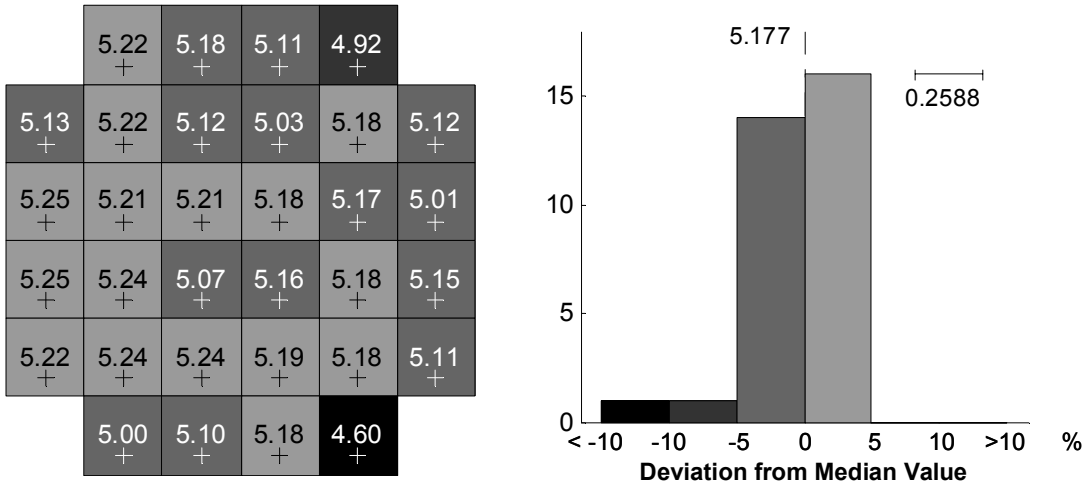


(b)

Figure B.16 Wafer map and distribution of (a) peak current (mA) and (b) PVCR for RTDs from Wafer 4243 with area $2 \times 2\ \mu m^2$.

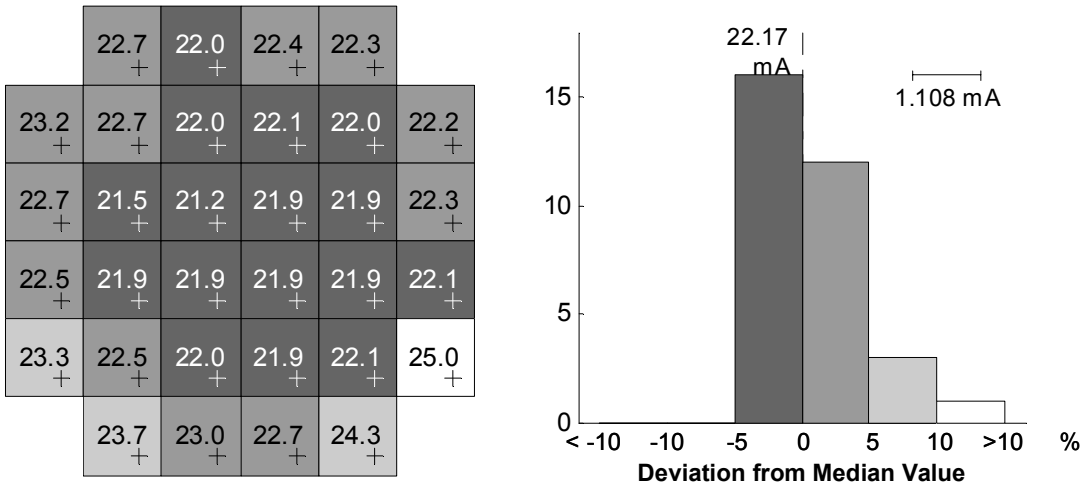


(a)

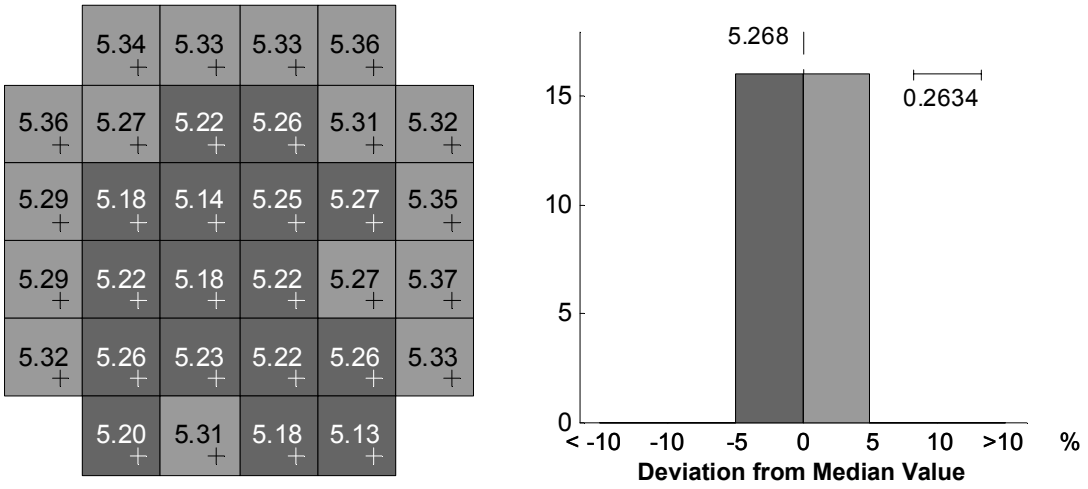


(b)

Figure B.17 Wafer map and distribution of (a) peak current (mA) and (b) PVCR for RTDs from Wafer 4243 with area $4 \times 4\ \mu m^2$.



(a)



(b)

Figure B.18 Wafer map and distribution of (a) peak current (mA) and (b) PVCR for RTDs from Wafer 4243 with area $6 \times 6\ \mu m^2$.

B.4. Statistical Distribution by Device Area

The statistical distribution of the peak current density (calculated from the measured peak current and nominal RTD area) and PVCR are shown in Figures B.19-B.24 for all three wafers tested. Between the different wafers, the main difference other than the intentional variation of peak current density is the higher PVCR evident in Wafer 4241 relative to the other wafers.

A common pattern among all three wafers is the imperfect scaling of the peak current relative to the nominal RTD area. If the true RTD current scaled perfectly, then the calculated peak current density would be the same for all nominal RTD areas. The data shown in Figures B.19, B.21, and B.23 indicate that the smaller RTDs have a higher peak current than would be expected if there were an ideal linear dependence of peak current with nominal area. There are two obvious ways in which the linear relationship between peak current and nominal area would be lost. The first such mechanism would be an excess current that does not scale with device area, presumably a surface leakage mechanism which scales with the perimeter-to-area ratio of the RTD. A surface leakage component to the peak current would explain the slightly higher than expected peak current in the 1.4×1.4 μm^2 and 2×2 μm^2 RTDs, but this hypothesis is contradicted by the lack of a reduction in PVCR with decreasing device area. An alternate explanation would be a discrepancy between the drawn RTD areas and the actual etched RTD areas. The most likely cause of such a discrepancy is a constant lateral etch undercut that gives rise to a larger relative reduction in RTD area in the small RTDs. Lateral undercut, however, would explain a decrease in nominal RTD peak current density with smaller drawn device areas, not an increase as observed. At present, this trend is not understood.

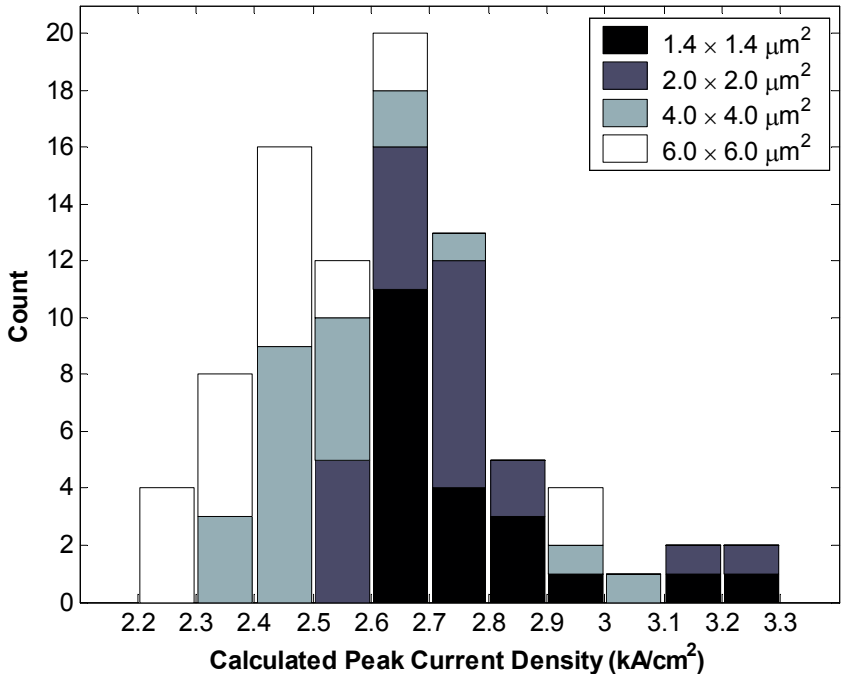


Figure B.19 Distribution of the peak current density for all functional RTDs from Wafer 4241 as calculated from the drawn RTD area and the measured peak current.

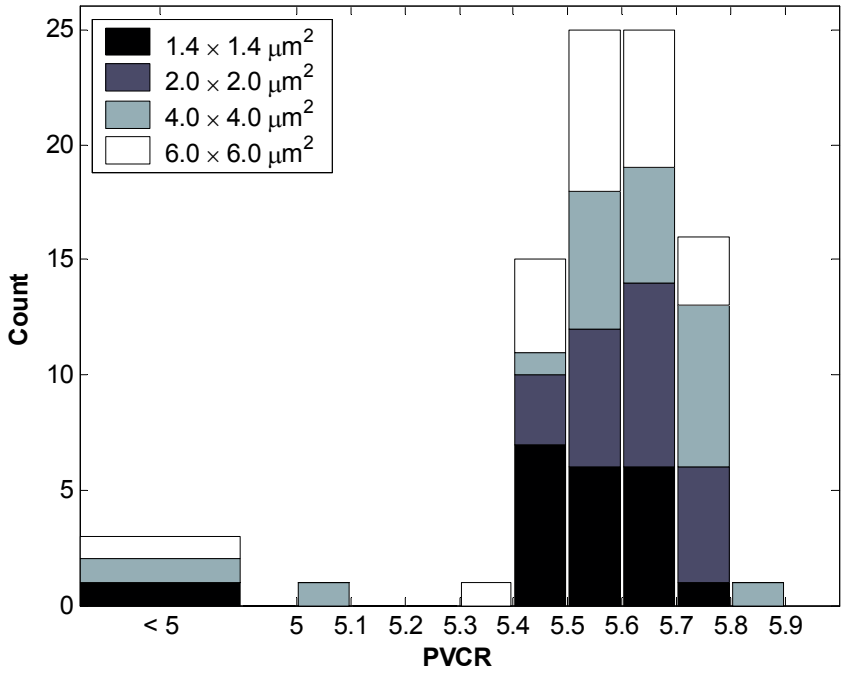


Figure B.20 Distribution of the measured PVCR for all functional RTDs from Wafer 4241.

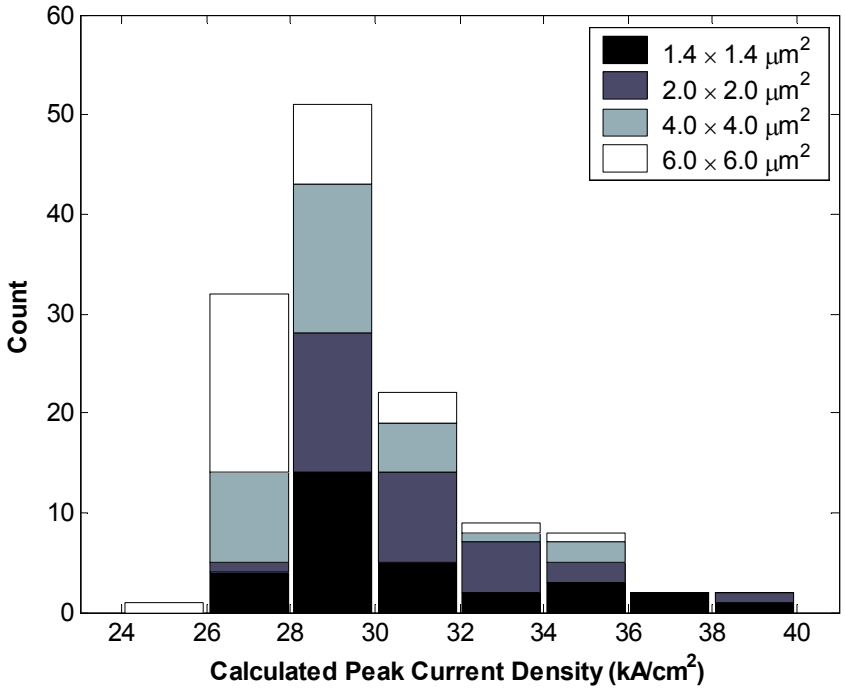


Figure B.21 Distribution of the peak current density for all functional RTDs from Wafer 4242 as calculated from the drawn RTD area and the measured peak current.

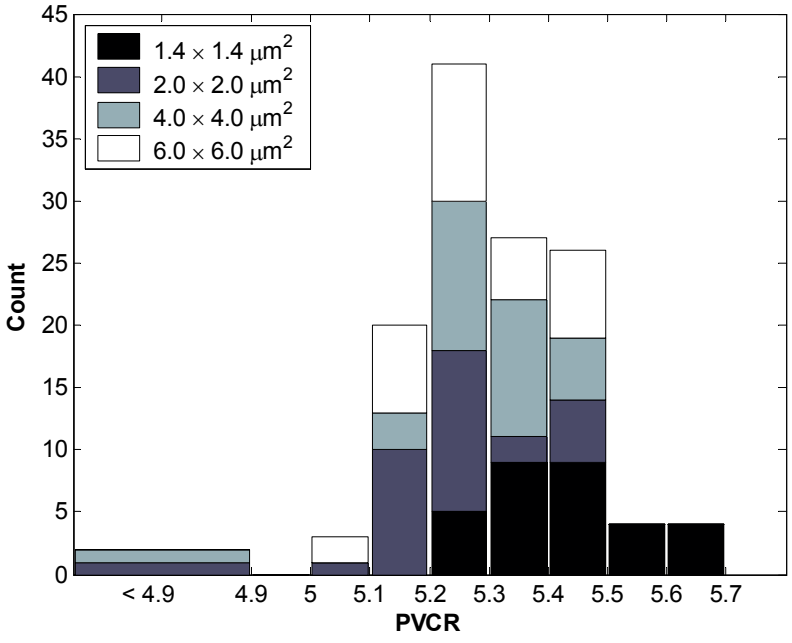


Figure B.22 Distribution of the measured PVCR for all functional RTDs from Wafer 4242

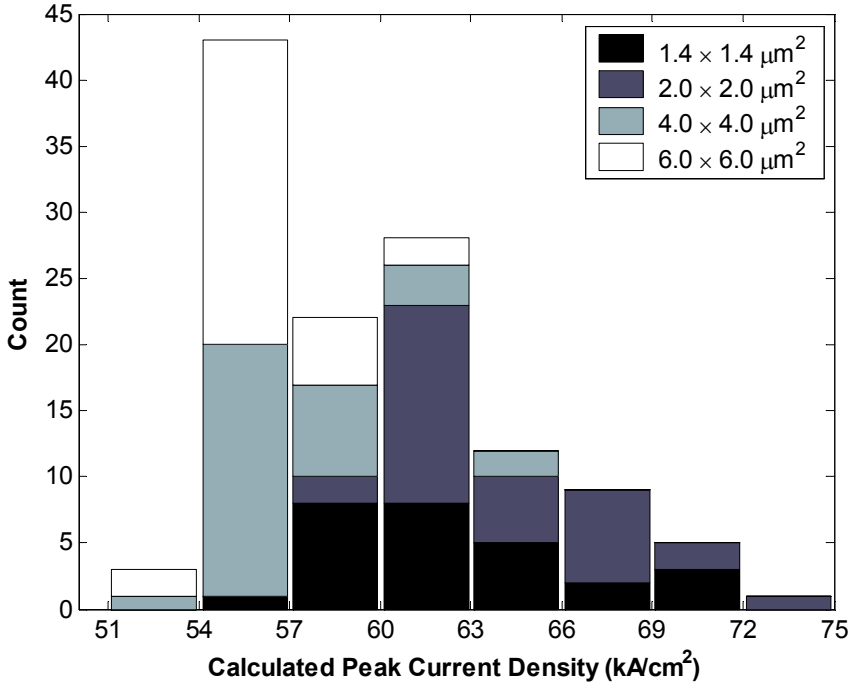


Figure B.23 Distribution of the peak current density for all functional RTDs from Wafer 4243 as calculated from the drawn RTD area and the measured peak current

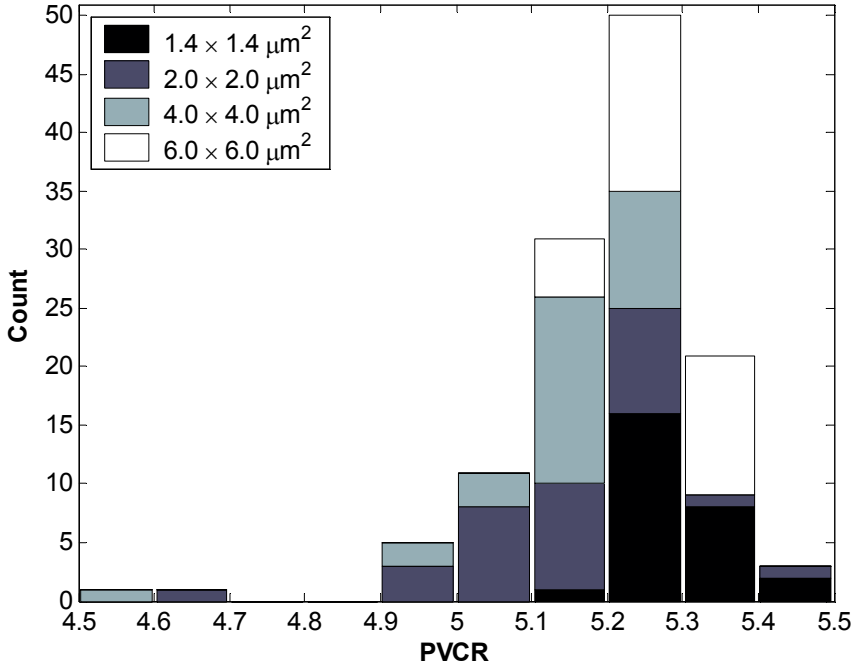


Figure B.24 Distribution of the measured PVCR for all functional RTDs from Wafer 4243.

Finally, for reference the a statistical summary of the peak current and voltage, valley current and voltage, and PVCR for all three wafers are tabulated in Table B.1-B.3. In general, the variances in the RTD electrical properties decreased with increasing device area with respect to RTDs on the same wafer. The peak and valley voltages generally had low statistical variations which were smaller than the measurement voltage resolution of 10 mV, which is expected because this parameter is determined primarily by the epitaxial layer structure and not the fabrication process. The effect of series resistance is observable in the upward shift of the peak voltage as the peak current increases.

Table B.1 Statistical summary of RTD electronic properties of Wafer 4241

Parameter		All Good Fields				Non-edge Fields			
		1.4 x 1.4	2 x 2	4 x 4	6 x 6	1.4 x 1.4	2 x 2	4 x 4	6 x 6
Number of Devices	Good / Total	21 / 22	22 / 22	22 / 22	22 / 22	11 / 12	12 / 12	12 / 12	12 / 12
Peak Current (mA)	Mean	0.073	0.145	0.539	1.175	0.072	0.139	0.520	1.122
	Median	0.073	0.144	0.532	1.159	0.073	0.140	0.519	1.111
	σ (mA)	0.0041	0.0092	0.0357	0.0851	0.0031	0.0056	0.0199	0.0445
	σ (%)	5.61%	6.38%	6.62%	7.24%	4.27%	3.98%	3.83%	3.97%
Valley Current (mA)	Mean	0.014	0.026	0.099	0.215	0.015	0.025	0.097	0.210
	Median	0.013	0.026	0.096	0.211	0.013	0.025	0.092	0.198
	σ (mA)	0.0050	0.0017	0.0150	0.0251	0.0070	0.0013	0.0189	0.0302
	σ (%)	35.35%	6.75%	15.22%	11.65%	46.04%	5.06%	19.41%	14.42%
Peak Voltage (V)	Mean	0.269	0.267	0.257	0.246	0.270	0.267	0.258	0.246
	Median	0.27	0.27	0.26	0.25	0.27	0.27	0.26	0.25
	σ (V)	0.0070	0.0070	0.0065	0.0073	0.0063	0.0049	0.0045	0.0067
	σ (%)	2.60%	2.63%	2.52%	2.95%	2.34%	1.85%	1.76%	2.72%
Valley Voltage (V)	Mean	0.558	0.556	0.554	0.564	0.555	0.556	0.553	0.562
	Median	0.56	0.56	0.55	0.56	0.56	0.56	0.55	0.56
	σ (V)	0.0089	0.0049	0.0059	0.0058	0.0121	0.0051	0.0065	0.0058
	σ (%)	1.59%	0.88%	1.07%	1.03%	2.18%	0.93%	1.18%	1.03%
PVCR	Mean	5.39	5.62	5.53	5.50	5.23	5.60	5.46	5.41
	Median	5.55	5.63	5.64	5.57	5.49	5.59	5.62	5.52
	σ	0.7561	0.0929	0.4882	0.3829	1.0330	0.0747	0.6311	0.5015
	σ (%)	14.02%	1.65%	8.83%	6.96%	19.77%	1.33%	11.57%	9.26%

Table B.2 Statistical summary of RTD electronic properties of Wafer 4242

Parameter		All Good Fields				Non-edge Fields			
		1.4 x 1.4	2 x 2	4 x 4	6 x 6	1.4 x 1.4	2 x 2	4 x 4	6 x 6
Number of Devices	Good / Total	31 / 32	32 / 32	32 / 32	32 / 32	15 / 16	16 /16	16 / 16	16 / 16
Peak Current (mA)	Mean	0.73	1.47	5.57	12.16	0.69	1.40	5.34	11.74
	Median	0.69	1.43	5.47	11.99	0.68	1.40	5.33	11.73
	σ (mA)	0.077	0.119	0.400	0.739	0.044	0.068	0.170	0.347
	σ (%)	10.53%	8.07%	7.18%	6.08%	6.34%	4.85%	3.18%	2.95%
Valley Current (mA)	Mean	0.135	0.282	1.100	2.306	0.128	0.273	1.010	2.234
	Median	0.128	0.271	1.024	2.271	0.126	0.268	1.003	2.223
	σ (mA)	0.015	0.024	0.331	0.125	0.008	0.019	0.037	0.044
	σ (%)	11.37%	8.37%	30.11%	5.40%	6.61%	7.06%	3.67%	1.97%
Peak Voltage (V)	Mean	0.235	0.236	0.252	0.266	0.236	0.234	0.251	0.264
	Median	0.24	0.24	0.25	0.26	0.24	0.23	0.25	0.26
	σ (V)	0.0051	0.0067	0.0055	0.0098	0.0051	0.0081	0.0034	0.0062
	σ (%)	2.16%	2.82%	2.19%	3.66%	2.15%	3.47%	1.36%	2.35%
Valley Voltage (V)	Mean	0.577	0.586	0.583	0.591	0.576	0.586	0.582	0.589
	Median	0.58	0.59	0.58	0.59	0.58	0.59	0.58	0.59
	σ (V)	0.0063	0.0055	0.0054	0.0053	0.0063	0.0051	0.0040	0.0044
	σ (%)	1.09%	0.94%	0.92%	0.90%	1.10%	0.87%	0.69%	0.75%
PVCR	Mean	5.43	5.22	5.22	5.27	5.38	5.14	5.29	5.25
	Median	5.41	5.23	5.29	5.26	5.39	5.20	5.29	5.26
	σ	0.1213	0.2167	0.5214	0.1192	0.0610	0.2645	0.0850	0.1104
	σ (%)	2.24%	4.15%	10.00%	2.26%	1.13%	5.14%	1.61%	2.10%

Table B.3 Statistical summary of RTD electronic properties of Wafer 4243

Parameter		All Good Fields				Non-edge Fields			
		1.4 x 1.4	2 x 2	4 x 4	6 x 6	1.4 x 1.4	2 x 2	4 x 4	6 x 6
Number of Devices	Good / Total	27 / 32	32 / 32	32 / 32	32 / 32	16 / 16	16 / 16	16 / 16	16 / 16
Peak Current (mA)	Mean	1.37	2.78	10.17	22.43	1.35	2.71	9.95	21.95
	Median	1.34	2.73	9.97	22.17	1.34	2.69	9.92	21.93
	σ (mA)	0.084	0.165	0.472	0.788	0.059	0.093	0.230	0.339
	σ (%)	6.12%	5.92%	4.64%	3.51%	4.32%	3.43%	2.32%	1.55%
Valley Current (mA)	Mean	0.259	0.542	1.983	4.258	0.257	0.528	1.922	4.194
	Median	0.256	0.537	1.949	4.203	0.256	0.522	1.916	4.193
	σ (mA)	0.014	0.039	0.125	0.152	0.009	0.021	0.046	0.049
	σ (%)	5.31%	7.28%	6.31%	3.56%	3.59%	3.96%	2.38%	1.17%
Peak Voltage (V)	Mean	0.212	0.218	0.231	0.262	0.211	0.217	0.231	0.261
	Median	0.21	0.22	0.23	0.26	0.21	0.22	0.23	0.26
	σ (V)	0.0042	0.0062	0.0034	0.0049	0.0034	0.0048	0.0034	0.0034
	σ (%)	2.00%	2.86%	1.45%	1.87%	1.62%	2.21%	1.48%	1.31%
Valley Voltage (V)	Mean	0.557	0.562	0.553	0.560	0.558	0.560	0.551	0.560
	Median	0.56	0.56	0.55	0.56	0.56	0.56	0.55	0.56
	σ (V)	0.0045	0.0071	0.0047	0.0000	0.0045	0.0063	0.0034	0.0000
	σ (%)	0.80%	1.26%	0.85%	0.00%	0.80%	1.13%	0.62%	0.00%
PVCR	Mean	5.29	5.14	5.14	5.27	5.26	5.14	5.18	5.23
	Median	5.28	5.15	5.18	5.27	5.24	5.15	5.18	5.24
	σ	0.0757	0.1537	0.1270	0.0663	0.0594	0.1006	0.0601	0.0416
	σ (%)	1.43%	2.99%	2.47%	1.26%	1.13%	1.96%	1.16%	0.80%

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